Manual

SOHARD
EMBEDDED SYSTEMS

SH IP-CORE-ARCCTRL

PM20100 Enhanced ARCNET Controller for FPGA-based designs

Version 02.02

CONTENTS

1 Revision history

Date	*Change*
July 10th, 2004	First released edition
September 1st, 2004	Support for Xilinx FPGA added
October 15th, 2004	EXNAK Function modified, Bridge Mode and Networklist functions and Messages added. Receive All Mode added (FPGA version >=V00.54)
V 00.33	New CMD for clearing interrupts (FPGA version >=V00.56)
V 00.34	Examples added
V 00.35	1-Wire Commands added, License Mode added, DID instead of Page Qualifier during packet reading (>=FPGA Version V00.64)
V 00.36	added Bit indicating the licensing status
V 00.37	various changes regarding licensing
V 00.38	various changes regarding licensing
V 00.39	various changes regarding licensing. MSG Codes added. CMD_DIS_PAC_RX added.
V 00.40	Wishbone Interface added
V 00.41	Node ID in Demomode is 0x0A, Codes for PAR_PM_ID_H added Commands CMD_SET_RAM_PRT_L and CMD_SET_RAM_PRT_H added
V 00.42	Some minor changes and cleanup.
V 00.43	New status (STS_PAGE Register) for manual abort added (FPGA version >=V00.84)
V 00.44	Minor changes & CI update
V 00.45	Minor changes
V 01.00	CI update
V 02.00	CI update
V 02.01	CMD_EN_TM and Recon Diagnostic Messages added (FPGA version >=V00.89) Faster Access from Hostcontroller (less waitstates for signal wait_ext)
V 02.02	License, Software and contact information updated

2 Overview

The PM20100 is an ARCNET [1] controller designed for Field-Programmable-Gate-Arrays (FPGA's). It has been written in VHDL and was designed for Altera FPGAs (Stratix, Apex, and Cyclone families) and Xilinx FPGAs (Spartan 3/3E, Virtex 2,4). The design contains some Altera/Xilinx Megafunctions like RAM's and FIFO's, which are clearly identified and have to be adopted if FPGAs of other vendors like are being used. Compared to classic „hardcoded“ chips, the PM20100 offers unlimited possibilities for the user to adopt the design to his needs.

2.1 Features

- fully compatible to ANSI/ATA 878.1 Local Area Network Standard for Arcnet
- up to 16 transmit/receive pages for long and short Arcnet packets
- bitrates adjustable from 19 kBps up to 30 Mbps
- automatic packet transmission abort after EXCNAK
- token auto-repeat
- improved network configuration
- enhanced diagnostic functions
- duplicate node detection
- simple register-based interface
- Receive-All Mode (option)
- Bridge function with virtual nodes (option)
- Complete network nodelist (option)
- “classic” bus interface or Wishbone interface available
- 1-Wire device for storage of various parameters and licensing (option)
- design entirely written in VHDL, exceptions are only RAM and FIFO functions
- may be easily adopted to other FPGA types
- in-field updates and upgrades are easy
- future proof
- free license for PM20100 in Demo Mode

2.2 Applications

Due to its high flexibility the design may be used for or adopted to a wide field of applications:

- One-Chip PCI Arcnet card (A free PCI Core is available from www.opencores.org)
- Simple and cost-effective node for versatile digital I/O
- Universal Arcnet-Arcnet or Arcnet-Ethernetbridge with virtual node-mapping
- Highspeed point-to-point connections
- Embedded networking
- System-On-Chip solutions

1 Hostinterface

The hostinterface is the interface to an external or internal microcontroller. It´s very similiar to a ISA-bus like interface with read, write, chipselect control signals, a 8-bit databus and a 4-bit adressbus. A Wishbone-compatible interface for SoC is available as well.

2.3 Registers

Only a few registers are required to take full control over the PM20100.

Registername	Address	Read/Write	Description
PAR	0	R/W	Parameter field for CMD. Must be set prior before executing a CMD which requires a parameter. Additionally this register returns the value of any CMD_GET_xx Command. Note: Writing this register disables the interrupt temporarily. The interrupt is enabled again, when the CMD register is written.
CMD	1	R/W	Writing to this register triggers various actions. See table of valid CMD Codes. The last executed command may be read back via this register.
PAGE_DATA	2	R/W	To fill a page for transmission, write the packet data to this register. The adresspointer for the page is incremented automatically with each write access to this register. Vice versa received packet data may be read via this register. The start address must be set to the initial value by executing a SET_PAGE command. A read access also increments the adress pointer automatically.
reserved	3	R/W	reserved
IRQ_STS_PAC	4	R	The status registers shows various events concerning packet receive and transmit. If enabled, each event causes an interrupt. Bit 3..0 contains the page, Bit 7..4 the events. See Table IRQ_STS_PAC
IRQ_STS_SYS	5	R	Various events like Reconfigurations, etc are shown here. If enabled, each event causes an interrupt. See Table IRQ_STS_SYS
MSG_PAR	6	R	Contains a parameter field for the MSG_NAME The MSG_PAR and MSG_Name registers are required for debugging purposes only. MSG_PAR must always be read after MSG_NAME.
MSG_NAME	7	R	The Message register is supplied by an internal FIFO. Reading the MSG_PAR updates the MSG registers with the next message. Messages deliver information on internal status of the controller, network events and responses to CMDs. See table.
reserved	8...F		reserved

All addresses are byte addresses.

2.3.1 Commands

By writing commands (and if necessary a parameter) the PM20100 performs the required actions like setting parameters, starting packet transmission, receiptions and so on. If the command requires a parameter, this parameter must be written first to the PAR register. After writing the command to the CMD register, the command ist executed.

Table: Valid commands and parameters

CMD Name	Command code in hex	Parameter	Description
CMD_SET_BITRATE	08	0...9	Sets the actual bitrate on the network. 0 corresponds to 19 kBps, 1 to 38 kBps,.. 7 to 2.5 Mbps and so forth up to 10 Mbps.(1),(3) Setting the bitrate automatically resets the internal statemachine.
CMD_SET_SID	01	1...FF	Sets the Node ID. Must be set prior to enabling the controller. In Demo-mode the CMD_SET_SID command is not being executed. This means the Node ID of the PM20100 is fixed to the default value (0x0A)
CMD_EN_ARC	38	xx	Enables network activity. The bitrate and the SID must have been set in advance. The PM20100 starts joining the network.
CMD_SET_TX_SID	19	1 .. FF	The SID of a packet to be transmitted may be set by this command. Refers to the page selected by the CMD_SET_PAGE Command. The command is available and necessary only, if the Bridge Mode option is enabled.
CMD_DIS_ARC	37	xx	Disables network transmission activity. Parameters are not changed. Packet transfers are being cancelled. Some monitoring activity is still running.
CMD_SET_PAGE	18	0..F	Sets the actual page. All subsequent CMDs regarding packet transfers refer to this page. Bit 0..3 of the parameter field indicate the page. Preparing a packet for transmission: First select the page (CMD_SET_PAGE). Then simply write the data to the PAGE_DATA register. DID, length and SID (in Bridge Mode only) must have been set by the approbiate commands before starting the actual transmission with a EN_PAC_TX command. To make sure that a previous transmission from this page has been completed, the status of the page should be evaluated first. Reading a received packet: The first byte read from the PAGE_DATA register is the STS_PAGE byte, followed by the lowbyte of length, SID, DID and the PAC data. To make sure the data is valid, the STS_PAGE register should be evaluated first. Please note, that the DID is not valid, if a broadcast packet has been received. Note: Writing to the page via the PAGE_DATA register *starts* (after CMD_SET_PAGE) always at an internal offset of 4 bytes referred to the beginning of the page. The first four bytes of the page are reserved for internal purposes for transmitting. Reading of the page via the PAGE_DATA register *starts* (after CMD_SET_PAGE) always at the beginning of the page. This must be taken in account, if a RAM test shall be performed
CMD_SET_RAM_PTR_L	1A	0..FF	Sets the internal pointer(low byte) for reading/writing the PAGE_DATA register to an arbitrary value. see command CMD_SET_PAGE. The CMD_SET_RAM_PTR_x commands may be used to write or read selected areas of a page.
CMD_SET_RAM_PTR_H	1B	0,1	Sets the internal pointer(high byte)
CMD_RST_ARC	44	xx	Resets the internal statemachine. All network activity is immediately stopped. All network relevant parameters (except bitrate) have to be set again. A minimum waiting time of 20us is required, before the next read/write access may occur.
CMD_SET_EXNAK	07	0...1F	Sets the value for FBE-NAK sequences, after which the EXNAK status bit is being set. A value for Bit 0..3 of 0 means disabled, 1 means 2 NAKs, 2 means 4 NAKs up to 15 which means 32768 NAKs. Bit 4 EXNAK auto abort option: If set, a running packet transmission is automatically aborted after EXNAK. If Bit 4 is cleared, only the EXNAK status bit is set, but the packet transmission continues.

CMD Name	Command code in hex	Parameter	Description
			Default after Power-up Or Reset is 128 NAKs and auto-abort disabled.
CMD_SET_IRQ_MASK_PAC	09	0..FF	Enables interrupt sources. See table for IRQ_MASK_PAC
CMD_SET_IRQ_MASK_SYS	0A	0..FF	Enables interrupt sources. See table for for IRQ_MASK_SYS
CMD_CLEAR_IRQ_SYS	0B	0..FF	Resets the IRQ_STS_SYS bits if the corresponding bit in the parameter field is set. The interrupt output is set inactive, if all bits in the IRQ_STS_SYS and IRQ_STS_PAC are cleared.
CMD_CLEAR_IRQ_PGE	0D	0..FF	Resets the IRQ_STS_PAC bits if the corresponding bit in the parameter field is set. The interrupt output is set inactive, if all bits in the IRQ_STS_SYS and IRQ_STS_PAC are cleared.
CMD_EN_PAC_TX	35	0..F	Enables a packet transmission and defines the selected page as an transmit page. All required parameters like DID, LEN and packet data must have been set before executing this command. The parameter field indicates the selected page. Be aware, that the actual transmission takes place only, when a eventually running transfer has been completed and no other pages have been enabled before. The packets are transmitted in the same order, as they have been enabled. See chapter PAGE_QUALIFIER
CMD_EN_PAC_RX	40	0..F	Enables a page for receiving and defines the selected page as a receive page. The parameter field indicates the selected page. Be aware, that the actual receiption takes place only, when a eventually running transfer has been completed and no other pages have been enabled before. The packets are stored in the selected page in the same order, as they have been enabled. See chapter PAGE_QUALIFIER
CMD_DIS_PAC_RX	41	0..F	Disables a page from receiving. The parameter field indicates the selected page. If the page was activated before for receive, the STS_PAGE Register will show an STS_PAC_RX_ABORT condition. Otherwise this register is cleared only.
CMD_RX_ALL_DIS	4F	--	Disables the Receive-All Mode. The command is available only, if the Receive-All option is enabled.
CMD_SET_PAC_LEN_L	05	0…FD	Sets the Lowbyte of the length of a data packet to be sent. Refers to the page selected by the CMD_SET_PAGE Command. Please keep in mind, that packet lengths of 254 – 256 and > 508 are not allowed.
CMD_SET_PAC_LEN_H	06	0…1	Packet Len is >= 257 byte (if set to 1), otherwise 1..253 according to the CMD_SET_PAC_LEN_H Command Refers to the page selected by the CMD_SET_PAGE Command.
CMD_SET_DID	02	0...FF	Sets the Destination ID for a packet transmission to another node in the network. 0 means the packet will be transmitted a a broadcast packet. Refers to the page selected by the CMD_SET_PAGE Command.
CMD_GET_PAGE_STS	27	0..F	Gets the actual status of a page. See table STS_PAGE. The parameter field indicates the selected page. The returned value shows up in the PAR Register
CMD_EN_BRDCST_RX	42	xx	Enables the controller to receive Broadcast packets. Default after reset is OFF.
CMD_DIS_BRDCST_RX	43	xx	Disables the controller to receive Broadcast packets.
CMD_RST_MSG_FIFO	45	xx	The FIFO containing MSGs is being reset.
CMD_ABORT_TX_PAC	36	xx	Aborts a packet transmission. This command is executed only if the actual PAC is not yet underway.
CMD_SET_TMR_TLT_L	10	0..FF	Sets the Lowbyte of the Token Lost Timer. The value is expressed in increments of 2048 bitlength. The register defaults to the standard timeout value (0x0401 = 840ms @2.5Mbps) [1]. The optimal value depends on the number of nodes in the network, the bitrate and the runtimes of the signal on the network lines. Please be careful to use the same timeout values on all nodes of the network.
CMD_SET_TMR_TLT_H	11	0..FF	Sets the Highbyte of the Token Lost Timer.
CMD_SET_TMR_TRP_L	16	0..FF	Sets the Low byte of the Response Timer. The value is expressed in increments of 0.5 bitlength. The register

CMD Name	Command code in hex	Parameter	Description
			defaults to the standard timeout value (0x017F = 76.6 us @2.5Mbps) [1]. The optimal value depends on the number of nodes in the network, the bitrate and the runtimes of the signal on the network lines. Please be careful to use the same timeout values on all nodes of the network.
CMD_SET_TMR_TRP_H	17	0..FF	Sets the Highbyte of the Response Timer
CMD_SET_TMR_TIP_L	12	0..FF	Sets the Low byte of the Identifier Precedence Timer. The value is expressed in increments of 0.5 bitlength. The register defaults to the standard timeout value (0x02DA = 146 us @2.5Mbps) [1]. The optimal value depends on the number of nodes in the network, the bitrate and the runtimes of the signal on the network lines. Please be careful to use the exact same timeout values on all nodes of the network.
CMD_SET_TMR_TIP_H	13	0..FF	Sets the Highbyte of the Identifier Precedence Timer.
CMD_SET_TMR_TAC_L	14	0..FF	Sets the Low byte of the Activity Timeout Timer. The value is expressed in increments of 0.5 bitlength. The register defaults to the standard timeout value (0x1A9 = 85 us @2.5Mbps) [1]. The optimal value depends on the number of nodes in the network, the bitrate and the runtimes of the signal on the network lines. Please be careful to use the same timeout values on all nodes of the network.
CMD_SET_TMR_TAC_H	15	0..F	Sets the Highbyte of the Identifier Precedence Timer.
CMD_GET_PARAM	29	See table Subcommands	This command allows to read back many values which have been set by CMD_SET_xx commands and some other interesting information. The value may be read from the PAR register.
CMD_SET_DEBUG_LVL	0C	0..FF	Defines which kind of MSGs are stored in the MSG FIFO. Default (00) is all MSGs enabled. Bit0=1: ignore ACK, NAK messages Bit1=1: ignore FBE messages Bit2=1: ignore messages of type MSG_ITT Bit3=1: ignore messages of type MSG_MY_ITT Bit4=1: ignore most messages except any kind of error message Bit5=1: ignore all network messages like MSG_TOKENPASS_FAIL, MSG_NEXTID_FOUND etc
CMD_SET_ENHNCD_MODE	48	0,1	Bit 0: Enables/disables the Token Repeat function. If enabled, the tokenpass will repeated once, if the first try has failed. If disabled, after a tokenpass failure the node searches for the next available node in the network as defined in [1]. Default is off. Bit 1..7 reserved for future enhancements
CMD_VN_EN_NODE	49	sid	Enables a virtual node. After this command the PM20100 acts like an Arcnet node with the node id given in the parameter field.(5)
CMD_VN_DIS_NODE	4A	1..FF	Disables a virtual node. (5)
CMD_VN_EN_RX	4B	1..FF	Enables a virtual node for receiving packets. (5) Note: To actually receive packets, the standard procedure for receiving packets (CMD_EN_PAC_RX etc.) has to be performed additionally.
CMD_VN_DIS_RX	4C	1..FF	Prevents a virtual node from receiving packets. (5) The virtual node always answers with NAKs on FBE queries.
CMD_REQ_NP_STS	4D	1..FE	Requests a Network nodelist. The PM20100 stores a list of nodestati (starting with the value given by the parameter field) in the Message Buffer. The number of messages is 8 maximum. The command is available only, if the Bridge Mode option or the Network Nodelist option is enabled.
CMD_DS_RP	60	--	Command for resetting the 1-Wire device. (4) The next CMD_DS_xx command may only be executed if the status of the the 1-Wire Device has been read.
CMD_DS_WRB	61	0..FF	Command for writing a byte into the 1-Wire Device. (4) The status of the command may be checked with the CMD_GET_PAR command with subcommand PAR_DS_STS.
CMD_DS_RDB	62	xx	Command for reading a byte from the 1-Wire device. (4) The status of the command may be checked with the CMD_GET_PAR command with subcommand PAR_DS_STS.
CMD_DS_CHK_LCS	63	xx	Starts the verification of the license. The PM20100 compares the information in the 1-Wire device with the license code and if successfull enables various features and functions. The verification works only, if the PM20100 is offline. Please wait about 50ms before accessing the PM20100 the next time. (4) In general

CMD Name	Command code in hex	Parameter	Description
			this comand is never needed because the PM20100 automatically performs the verifification after power-up or a reset. Whether the verification process was successfull may be checked with the CMD_GET_PAR (subcommand PAR_SYS_RSRC) command. For more details see chapter "Licensing"
CMD_EN_TM	46	xx	Enables various features for testing an Arcnet network. Par=0x01: The next transmitted packets is sent with wrong CRC Par=0x02: The next Token to this node is ignored. This causes a reconfiguration sooner or later other functions tbd
	reserved	xx	Reserved for further enhancements

(1) depends on the actual FPGA and the used clock frequency.
(2) xx means Don´t Care.
(3) All timing values and bitrates refer to an external clock of 40 Mhz.
(4) All CMD_DS_xx commands are available only, if the license option is available. After executing a CMD_DS_xx command the status must be read before the next CMD_DS_xx command may be executed. Page 0 and 1 of the 1-Wire Device are reserved for license checking. Page 2 and 3 may be programmed with user data.
(5) The command is available only, if the Bridge Mode option is enabled

2.3.1.1 Subcommands

Subcommands are used for the CMD_DS and the CMD_GET_PAR commands.

Table: Subcommands for the CMD_GET_PARAM command

Subcommand Names	Sub-command value in hex	Description
PAR_EXNAK	7	Value see CMD_SET_EXNAK command
PAR_BITRATE	8	The adjusted bitrate.
PAR_NID	1	The Node Id of this node.
PAR_IRQ_MASK_PAC	9	Value see CMD_SET_IRQ_MASK_PAC command
PAR_IRQ_MASK_SYS	A	Value see CMD_SET_IRQ_MASK_SYS command
PAR_NEXTID	39	The Next ID of this node in the network. If 0, no neigbhbour node exists or the network is currently in the configuration process.
PAR_NWRK_STS	3A	Bit 0 = 1 indicates a node in the network with the same Node ID as this one. In this case the command CMD_EN_ARC should never be executed, because duplicate nodes may cause big trouble in a network. Bit 1= 1 means no activity in the network i.e. no other node is active Bit 2 =1 means a network with only one node has been detected Bit 3 = 1 means some tokens have been seen All Bits are reset by a CMD_DIS_ARC, CMD_SET_SID or CMD_RST_ARC command. Bit 4 = 1 means the network is stable (non configuring). The bit is valid only, if the Bridge Mode option or the Network Nodelist option is enabled.
PAR_FPGA_VENDOR_ID	40	Describes the Vendor of the FPGA. 0 = Altera, 1= Xilinx, 2= Actel, others are tbd.
PAR_FPGA_FAMILY_ID	41	Describes the FPGA Family. 0 = Cyclone, 1= Stratix, 2 = Apex (Altera), 3 = Cyclone II 0 = Spartan, 1 = Virtex (Xilinx)
PAR_PM_ID_L	42	The individual product ID (lowbyte) for the customer the PM20100 was compiled for. 00 = unknown
PAR_PM_ID_H	43	The individual ID (highbyte) for the customer the PM20100 was compiled for. 00 = prototypes, 01 = Sohard Embedded Systems GmbH, 02 = Siemens AG, 03= MEN, 04= Vestas, others tbd.
PAR_VER_MAJOR	44	Version, Highbyte
PAR_VER_MINOR	45	Version, Lowbyte
PAR_NR_OF_PAGES	46	Indicates the number of TX/RX pages available. The maximum value is 16 and depends on the FPGA the design was compiled for.
PAR_ENHNCD_MODE	48	Bit0: If 1 the Token Repeat function is enabled. See CMD_SET_ENHCD_FCKTS. Bit1..7 = 0 (reserved)
PAR_DS_STS	4A	The status of the CMD_DS_xx commands. Bit0..3 = 0: Idle 1: command still busy 2: command executed and ok 3: error (i.e. 1-wire device not present, error during reading/writing)
PAR_DS_RDB	4B	The value read back from the 1-Wire device with the CMD_DS_RDB command. Only valid if the status of the command is ok.

Subcommand Names	Sub-command-value in hex	Description
PAR_NWRK_STS	3A	Bit 0 = 1 indicates a node in the network with the same Node ID as this one. In this case the command CMD_EN_ARC should never be executed, because duplicate nodes may cause big trouble in a network. Bit 1= 1 means no activity in the network i.e. no other node is active Bit 2 =1 means a network with only one node has been detected Bit 3 = 1 means some tokens have been seen All Bits are reset by a CMD_DIS_ARC, CMD_SET_SID or CMD_RST_ARC command. Bit 4 = 1 means the network is stable (non configuring). The bit is valid only, if the Bridge Mode option or the Network Nodelist option is enabled.
PAR_SYS_RSRC	47	Bit0: Message Fifo enabled/disabled Bit1: CMD_SET_TMR_xx commands enabled (if disabled always the built-in default values are being used) Bit2: Network Status detection enabled/disabled Bit3: Enhanced Mode functions enabled. See CMD_SET_ENHNCD_MODE command. Bit4: Fast Host interface. The interface is clocked with the external clock(1), otherwise with half the external clock(0) Bit5: Bridge Mode. If 1 the Bridge Mode is enabled and virtual nodes are available Bit6: Network Nodelist. The complete ntwork nodelist is available via CMD_REQ_NP_STS commands. Bit7: Demo Mode. In Demo mode the CMD_SET_SID command is not beeing executed. This means the node id of the PM20100 is fixed to the default value (0x0A). 1 means enabled, 0 disabled.
PAR_SYS_RSRC1	49	Bit0: Receive-All Mode enabled/disabled Bit1: Licensing via 1-Wire Chip enabled/disabled Bit2: A correct licensecode was detected Bit 3..7: reserved 1 means enabled, 0 disabled.

2.3.2 Status registers

The status register shows events happened. If enabled by the SET_IRQ_MASK_PAC or SET_IRQ_MASK_SYS command the event causes an interrupt.

2.3.2.1 IRQ_STS_PAC Register

Name	Bit	Description
page	3..0	The page number to which the event refers.
PAC_TX_END	4	The transmission of a packet has been completed. Whether the transmission was successfull or not may be retrieved via the CMD_GET_PAGE_STS command.
PAC_RX_END	5	A data packet has been received. Whether the reception was successfull or not may be retrieved via the CMD_GET_PAGE_STS command.
reserved	6..7	reserved

Each bit may be reset individually by a CMD_CLEAR_IRQ_PGE command, if the corresponding bit in the parameter field is set.

2.3.2.2 IRQ_STS_SYS Register

Event	Bit	Description
RECON	0	A Reconfigurationburst has been triggered by this controller.
NEW_NEXT_ID	1	A new Next ID has been detected.
PAC_TX_EXNAK	2	During transmission of a packet the predefined value of NAKs has beeen received.
MSG_BUF_HALF	3	The message buffer is half full
MSG_ERROR	4	A MSG which shows an error or warning has been stored in the Message FIFO.
NO_ACTIVITY	5	A “No Activity” condition has been detected. Usually occurs s after a reconfiguration burst.
NW_CHANGE	6	The network nodelist has changed. The function is available only, if the Bridge Mode option or the Network Nodelist option is enabled.
reserved	7	reserved

Each bit may be reset individually by a CMD_CLEAR_IRQ_SYS command, if the corresponding bit in the parameter field is set.

2.3.3 IRQ MASK Registers

The interrupt mask registers enable or disable the various interrupt sources. They are controlled by the CMD_SET_IRQ_MASK_PAC / CMD_SET_IRQ_MASK_SYS commands.

2.3.3.1 IRQ_MASK_PAC Register

Name	Bit	Description
reserved	0..3	
PAC_TX_END	4	Enables Interrupt for the following event: A transmission of a packet has been completed.
PAC_RX_END	5	Enables Interrupt for the following event: A packet has been received
reserved	6..7	

2.3.3.2 IRQ_MASK_SYS Register

Event	Bit	Description
RECON	0	Enables Interrupt for the following event: A Reconfigurationburst has been caused by this controller.
NEW_NEXT_ID	1	Enables Interrupt for the following event: A new Next ID has been detected
PAC_TX_EXNAK	2	Enables Interrupt for the following event: During a transmission of a packet the predefined value of NAKs has beeen received.
MSG_BUF_HALF	3	Enables Interrupt for the following event: The message buffer is half full
MSG_ERROR	4	Enables Interrupt for the following event: A MSG which shows an error or warning has been stored in the Message FIFO
NO_ACTIVITY	5	Enables Interrupt for the following event: A “No Activity” condition has been detected. Usually occurs after a reconfiguration burst.
NW_CHANGE	6	Enables Interrupt for the following event: The network has become stable or has become instable (i.e. configuring). The function is available only, if the Bridge Mode option or the Network Nodelist option is enabled. May be used to trigger a readout of the network nodelist via the CMD_REQ_NP_STS command.
reserved	7	

2.3.4 STS_PAGE Register

After a CMD_GET_PAGE_STS command the status of a page may be readout via the PAR register. The table shows the possible status values. The status bits have different meanings if used as either an TX page or a RX page.

Table: STS_PAGE Register if configured as transmit page (PAGE_MODE Bit is set)

Name	Bit	Value in hex	Description
PAC_LEN	0	0,1	0 means the packet contains 1..253 Byte of data, 1 means the packet length is >=257 bytes
PAGE_MODE	1	1	Page is configured as TX page
EN_PAGE	2	0,1	Page is enabled for transmit when set to 1
STS_IDLE	5..3	0	Reset value. If EN_PAGE is set, the page is now waiting for being activated.
STS_PAC_PENDING	5..3	1	The page has been activated and will be transmitted as soon the receiving node is ready for receiving.
STS_PAC_TX_OK	5..3	2	A packet has been transmitted successfully
STS_FBE_TIMEOUT	5..3	3	A timeout after a FBE has occurred
STS_PAC_TIMEOUT	5..3	4	A timeout after a PAC has occurred
STS_PAC_ABORT	5..3	5	The packet transmission has been aborted by command or by reaching the number of adjusted NAKS, if the EXNAK auto abort option is enabled.
STS_PAC_ERROR	5..3	6	During the transmission of a packet an error has been detected and the transmission therefore has been aborted
STS_PAC_EXNAK	5..3	7	The number of NAKS set by the SMD_SET_EXNAK Command has been reached. If the auto abort option is enabled an Abort Command will be issued. The status value is overwritten when the packet transmission has been completed (OK, Timeout, or Error).
reserved	6..7	-	Used for internal purposes

Table: STS_PAGE Register if configured as receive page (PAGE_MODE Bit is cleared)

Name	Bit	Values in hex	Description
PAC_LEN	0	0,1	0 means the packet contains 1..253 Byte of data, 1 means the packet length is >=257 bytes
PAGE_MODE	1	0	Page is configured as RX page
EN_PAGE	2	0,1	Page is enabled for receive when set to 1
STS_PAC_RX_IDLE	5..3	0	Reset value. If EN_PAGE is set, the page is now waiting for being activated.
STS_PAC_RX_PENDING	5..3	1	The page has been activated to receive the next incoming data
STS_PAC_RX_BUSY	5..3	2	The page is currently being filled with received data
STS_PAC_RX_ERROR	5..3	3	An error occurred during receiving
STS_PAC_RX_OK	5..3	4	A packet has been received successfully
STS_PAC_RX_ABORT	5..3	5	A packet receive has been aborted manually by a CMD_DIS_PAC_RX command
STS_PAC_RX_BRDCST	6	0,1	If set, a Broadcast packet was received
reserved	7	-	Used for internal purposes

All status values are automatically reset by a CMD_EN_PAC_TX or CMD_EN_PAC_RX Command.

2.3.5 Page Queuing

If several pages for transmit or receive are in operation (are enabled) at the same time, it is important to know the sequence of enabling. Otherwise the sequence of packets may get wrong. The PM20100 fully takes care of this problem.
The pages are always filled with received data in the exact same order as the pages have been enabled. Vice versa packets are transmitted in the same order as they have been enabled. Interrupts indicating the completion of a PAC receive or transmission are generated in exactly the same sequence.

For example: Page 4, 2 and 7 are enabled one after the other by the CMD_EN_PAC_RX command. The first received packet is then stored in page 4, the second in page 2 and the third one in page 7.

2.4 Messages

To ease debugging a message buffer is provided. For normal operation the message buffer may be ignored or disabled.
The message buffer is a FIFO, which contains all internal messages generated by internal functions. By reading the register, the next stored message will appear. If the MSG name field has the hex value 00, the FIFO is empty.
Note: If the FIFO becomes full, new arriving messages are ignored. The type of messages stored in the FIFO may be controlled by the debug level. Please keep in mind, that the response to a command may be delayed, because the command has to be processed internally which may take a while.
The Parameter field contains further information. The used codes for the Messages (MSG) are the same as the codes for Commands (CMD).

Table: Messages

MSG Name	Value in hex	Parameter	Description
CMD_xx	--	Command-status	Most commands listed in the Command table deliver a status value, which indicates the status after execution. See tables "Commands" and "Command Status"
MSG_RECON_TRANSMITTED	50	--	The controller has sent a reconfiguration burst
MSG_NEXTID_FOUND	51	NID	The controller has found a new neiighbour in the network with the node id NID
MSG_DID_ERROR	52	--	An ITT send to this controller has a wrong DID
MSG_HEADER_LEN_ERROR	53	--	The start of a received arcnet frame has the wrong length
MSG_MY_FBE_RECEIVED	54	DID	A FBE to this node has beeen received
MSG_ACK_SENT	55	--	An ACK has been sent by this node
MSG_MY_ACK_RECEIVED	56	--	An ACK has been received and directed to this node
MSG_NAK_SENT	57	--	A NAK has been sent by this node
MSG_MY_NAK_RECEIVED	58	--	A NAK has been received and directed to this node
MSG_TOKENPASS_FAIL	59	--	The Token could not been passed to another node
MSG_TIMEOUT	5A	--	A timeout occurred after transmission of an Arcnet frame.
MSG_PAC_RX_SID	5B	SID	The SID of a received packet
MSG_PAC_RX_DID	5C	DID	The DID of a received packet
MSG_PAC_RX_LEN_L	5D	Length lowbyte	The length of a received packet (Lowbyte)
MSG_PAC_RX_LEN_H	5E	Length High	The length of a received packet (Highbyte)
MSG_PAC_RX_CRC_OK	5F	--	The CRC of a reveived packet is ok.
MSG_PAC_RX_CRC_ERROR	60	--	The CRC of a reveived packet is corrupt
MSG_PAC_NO_CRC	61	--	The received packet did not contain a CRC
MSG_PAC_RX_LEN_ERROR	62	--	The received packet did not contain enough data
MSG_PAC_TX_LEN_ERROR	63	--	The transmitted packet did not contain enough data
MSG_PAC_TX_OK	65	--	The transmitted packet has successfully been transmitted
MSG_PAC_TX_TMT	66	--	A timeout occurred after a transmitted packet
MSG_FBE_TX_TMT	67	--	A timeout occurred after a sent FBE
MSG_PAC_TX_STARTED	68	--	The packet transmission has started.
MSG_RX_UNKNOWN_ELEMENT	69	FID	The received Arcnet frame could not be identified as a valid Arcnet frame
MSG_FIFO_2ARC_FULL	6A		The internal FIFO to the statemachine is full. Command had to be ignored.
MSG_NO_ACTIVITY	6B		A Timeout (TAC Timer) has occurred, which means a Reconburst has beeen triggered by anode on the network.
MSG_ITT	6F	DID	An ITT directed to another node has been detected

MSG Name	Value in hex	Parameter	Description
MSG_MY_ITT	70	SID	An ITT directed to this node has been detected. In Bridge Mode the SID is variable, otherwise fixed
MSG_TMT_ITT	71	0	A Timeout after an ITT has been sent was detected
MSG_FBE_SENT	72	0	A FBE has been transmitted
MSG_PAC_TX_GEN_ERROR	73	0	An error after a PAC transmission has been detected
MSG_PAC_RX_GEN_ERROR	74	0	An error during a PAC receiption has been detected
MSG_NP_STATUS	75	0..FF	The message is generated if a CMD_REQ_NP_STS has beed executed. Bit0: If set the node is present and it is a “real” one Bit1: If set the node is present and it is a virtual node Bit2: If set the virtual node is enabled for receiving. Bit 3,4: If > 0 the node is present and a real one. If Bit 0,1 are cleared, the node is not adjacent to any of the PM20100´s real or virtual nodes. Non present nodes are not shown. The command is available only, if the Bridge Mode option or the Network Nodelist option is enabled.
MSG_NP_NXTID	76	1..FF	Indicates the id of neighbour node. This messages always follows a MSG_NP_STATUS message and is linked to it. A maximum of 8 messages are issued, if a CMD_REQ_NP_STS is executed. The netlist is valid only if a MSG_NW_STABLE message has been detected before. To ensure the validity of the network nodelist, perform a check if all MSG_NP_NXTID values together show a non-broken chain of next ids.
MSG_NW_NOT_STABLE	77	xx	The Network has started changing. For example, if a node has gone out of the network or a Reconburst has been issued. The command is available only, if the Bridge Mode option or the Network Nodelist option is enabled.
MSG_RECON_RCVD	7A	0..FF	A reconfiguration burst has been received from another node. The transmitted value is the Node-Id or zero if the transmitting node could'nt be identified.
MSG_RECON_VERSION	7B	0..FF	A reconfiguration burst with diagnostic data attached has been received from another PM20100. The transmitted value is the the version (PAR_VER_MINOR).
NULL	0	xx	The FIFO is empty, i.e. no messages are available

Table: Commandstatus

Commandstatus	Value in hex	Description
CMD_STS_OK	2	The command was successfully executed
CMD_STS_UNKNOWN	9	An invalid command has been detected and ignored.
CMD_STS_REJECTED	4	The command is valid, but could not be executed due to the internal state. For example: The CMD_EN_ARC Command is rejected, if the SID has not yet been set.
-	All other values	Reserved

3 Licensing

For questions on licensing options please contact info@sohard.de or any SOHARD sales representative.

4 Bridge Mode

The Bridge Mode is an advanced feature which allows the user to couple different Arcnet networks (different means for example different bitrates, timing settings, number of nodes, etc) in a transparent way. This is being done by the means of virtual nodes.

Real nodes in one network are represented by virtual nodes (implemented by the PM20100) in the other network. A link of any kind (Ethernet with TCP/IP protocol, modem lines, RS232, etc) then connects the Arcnet networks. A Bridge (containing a PM20100, a processor and a Bridge SW) in each Arcnet network may do the job to control the virtual nodes.

Example:

A node with NID=1 in network A for example likes to send a packet to a Node with NID=2 in network B. The bridges in Network A/B then automatically enable a Virtual Node with NID=2 in network A and a Virtual Node with NID=1 in network B.

The node with NID=1 in network A then sends ist packet to the Virtual Node with NID=2 in network A. The data is transferred from Bridge A to Bridge B. The Virtual Node with NID=1 in network B then sends the Arcnet data to the Node with NID=2 in network B.

The Bridges must manage the enabling/disabling of the Virtual nodes according to the status of the corresponding nodes in the other network, the communication between the bridges, the queuing of packets and so on.

5 Input/Output Pins

There are several groups of signals available. They are divided in system pins (clock, reset, leds, 1-wire), pins for connection the arcnet transceiver (rx, txenable etc.), pins to connect to an external microcontroller or to an internal FPGA based controller via Wishbone Interface[5].

5.1 System Interface

Table: Pins

Pinname	Direction	Description
clock	I	The central clock for all arcnet related All bitrates and timing values refer to a clock of 40 MHz. Without internal PLL a maximum bitrate of 10 MBps is achieved. For higher bitrates a PLL may be used, which may be driven by this clock. Also the clock for the classic interface to an external microcontroller
reset	I	Resets all internal logic except the Wishbone interface and the Internal Ram
int	O	Active high interrupt
nled_hst	O	Output for a led. Each access (read or write) to to PM20100 triggers the led for about 3 ms.
nled_act	O	Output for a led. Acitivity on the rx pin triggers the led. The on-time of the led depends on the selected bitrate.
ds_1wire	IO	data line to a 1-Wire device like the DS2431. See [4]

Note: O= Push-Pull Output, I = Input, IO = Input/Output

5.2 Arcnet Interface

For the transceiver interface the following pins are provided:

Table: Pins

Pinname	Direction	Description
rxin	I	The receive data from the network. Must be Active high
npulse1	O	The /pulse1 output for ARCNET coax transveivers
npulse2	O	The /pulse2 output for ARCNET coax transveivers
ntxdata	O	The /txdata output to ARCNET transveivers like RS485 and fibre optics
tx_en	O	Enables the ARCNET transceiver for transmitting
d2clk	O	bitrate clock x 2
d4clk	O	bitrate clock x 4

Note: O= Push-Pull Output, I = Input, IO = Input/Output

5.3 Classic Interface

For the interface to an external microcontroller the following pins are provided:

Table: Pins

Pinname	Direction	Description
nrd	I	The nrd signal from the microcontroller for read accesses. Active Low.
nwr	I	The nwr signal from the microcontroller for write accesses. Active Low.
wait_ext	O	High indicates that the host should extend the read/write cycle until wait_ext goes Low again.
ncs	I	The ncs signal from the microcontroller. Enables write/read accesses. Active Low.
oe_ext	O	Output enable for databus (High during read access). May be used to enable a tristatebuffer
data_frmext[7..0]	I	Databus from host to PM20100.
data_2ext[7..0]	O	Databus from PM20100 to host
adr_ext[3..0]	I	Addressbus from host

Note: O= Push-Pull Output, I = Input, IO = Input/Output

Note: The nwr and nrd strobes must be at least 450ns long (40 MHZ Clock), if the wait_ext pin is not being used. The wait pin delivers a signal which starts max.100 nsec later than a valid rd/wr access starts. The idle time after an access (ncs = High) should be at least 25 ns before the next access starts. If the host watches the wait_ext signal as described a mean access time for a read/write cycle of about 300ns may be reached. The host controller can end the bus cycle as soon as wait_ext goes Low again.
The data and address lines must be valid when nwr goes Low.

5.4 Wishbone Interface

Table: Pins

Pinname	Direction	Description
clk_i_wb	I	The clock for the synchronous Wishbone Interface.
rst_i_wb	I	Resets the Wishbone Interface
cyc_i_wb	I	Indicates a Wishbone Bus cycle.
we_i_wb	I	Indicates if the current bus cycle is a write or a read cycle
strb_i_wb	I	Addresses the PM20100 and starts the bus cycle
adr_i_wb[3..0]	I	Adress from Wishbone Master.
data_i_wb[7..0]	I	Data from Wishbone Master.
data_o_wb[7..0]	O	Data to Wishbone Master.
ack_o_wb	O	Indicates the PM20100 has completed the bus cycle (i.e. has registered the written data or delivered read data)

Note: O= Push-Pull Output, I = Input, IO = Input/Output

Note: The PM20100 always acts as a Wishbone Slave with single 8-Bit read/write cycles.
For a detailed description of all Wishbone Interface Signals please see [5].

6 Implementation

6.1 Altera FPGAs

6.1.1 Development Tool

The design was developed with the Altera Quartus 9.0 (or higher) Web Edition. This tool may be downloaded from www.altera.com for free.

6.1.2 Ressources

The following table gives a rough overview how many ressources the design requires. The values refer to the Altera Cyclone Family. Various options are available to reduce the ressource count. All values refer to the used Altera Software Quartus 6.0 Web Edition.

Table: Ressource count

Configuration	Ramblocks (512 byte size)	Logic Cells (LC)
Design with all functions (except Bridge Mode and Network Nodelist) enabled NR_OF_PAGES = 16	23	approx 4250 LCs
„Minimal“ design: NR_OF_PAGES = 2, MSG Buffer disabled, CMD_SET_TMR_xx commands disabled, Network status disabled, Enhanced Mode functions disabled, Receive-All Mode disabled	7	approx 4000 LCs
MSG Buffer disabled	Saves one ram block compared to the „full“ version“	Saves approx 80 Lcs compared to the „full“ version“
CMD_SET_TMR_xx disabled	0	Saves approx 150 LCs compared to the „full“ version“
Network status detection disabled	0	Saves approx 60 LCs compared to the „full“ version“
Network Nodelist without Bridge Mode	1	Approx 700 LCs compared to the „full“ version“
Receive All Mode	1	Approx 40 LCs compared to the „full“ version“
Bridge Mode (encompasses the Network Nodelist option as well)	2	Approx 900 LCs

Notes:

Each TX/RX page requires one RAM block of 512 byte size.

6.1.3 Performance

The timing simulation shows that the PM20100 can generate bitrates up to 20 Mbps with a FPGA of type EP1C6T144-8. To achieve these values an external clock of 80 Mhz is required. The design may better use an internal PLL to achieve higher bitrates than 10 Mbps (not yet implemented).

Note: The maximum datarate supported by standard Arcnet controllers like the COM20022 [2] is 10 MBps.

6.2 Xilinx FPGAs

6.2.1 Development Tool

The design was developed with the Xilinx ISE 11.2 (or higher) Webpack Version. This tool may be downloaded from www.xilinx.com. The tool is for free.

6.2.2 Ressources

The following table gives a rough overview how many ressources the design requires. The values refer to the Xilinx Spartan 3 Family. Various options are available to reduce the ressource count.

Table: Ressource count

Configuration	Ramblocks (18Kbit size)	Slices
Design with all functions (except Bridge Mode and Network Nodelist) enabled NR_OF_PAGES = 16	5	approx. 2510 (70% of a XC3S400xx)
„Minimal“ design: NR_OF_PAGES = 4, MSG Buffer disabled, CMD_SET_TMR_xx commands disabled, Network status disabled, Enhanced Mode functions disabled	2	approx. 2140

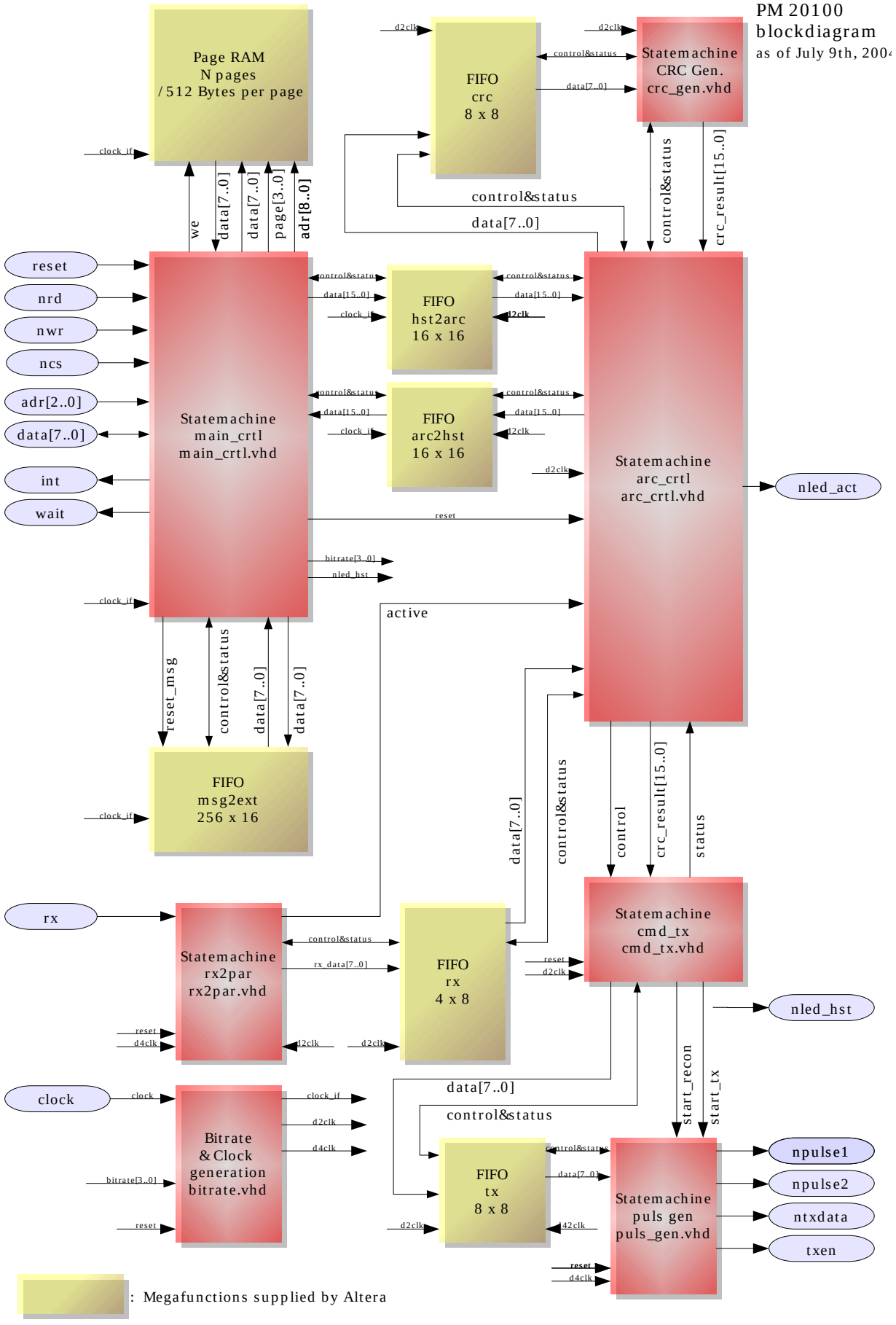
Note: 4 TX/RX page require one RAM block of 18 kbit size.

7 Technical background information

7.1 Overview

The design has been completely written in VHDL. Altera/Xilinx provide some functions like RAMs and single clocked FIFOs. These components have to be replaced by equivalent functions if other non-Altera/Xilinx FPGAs are to be used.

7.2 Block diagram Altera FPGAs



Notes:

- d2clk is a clock 2-times faster than the bitrate
- d4clk is a clock 4-times faster than the the bitrate
- clock_if is a clock for the external interface (20 or 40 Mhz and fixed)

7.3 Design units

design unit	description
main_crtl	ram control interface between external and arc_crtl interrupt and status generation
arc_crtl	controls all network operations
bitrate	generates clocks d2clk, d4clk and clock_if
puls_gen	serializes parallel data for transmission
cmd_tx	controls transmission of all Arcnet frames
crc_gen	computes the CRC for PAC transmission and receive
rx2par	serializes the received data and converts it to a 8-bit parallel datastream
np_crtl	keeps a list of all nodes in the network and their stati. Only used if the Bridge Mode or Nodelist Map option is enabled.
rdwr_1wire	controls the 1-Wire device. Only used, it the License option is enabled
FIFO msg2ext	FIFO with single clock. Stores the messages provided for debugging purposes.
FIFO rx	FIFO with single clock. Stores the received data.
FIFO hst2arc	FIFO with seperated clocks for reading and writing. Stores the commands for arc_crtl.
FIFO arc2hst	FIFO with seperated clocks for reading and writing. Stores messages for main_crtl.
FIFO tx	FIFO with seperated clocks for reading and writing. Stores the data to be transmitted
Page RAM	RAM where the reveived data and the data to be transmitted is stored. Each page requires 512 Bytes. Up to 16 pages (depending on available ressources) may be used.

Note: All FIFOs are standard Megafunctions provided by Altera and included in the QUARTUS Software package.

The blockdiagramm for Xilinx FPGAs is almost identical and therefore not shown here. The only exceptions are the depth of the FIFOs and the RAM (one block ram contains 4 RX/TX pages and has 18kbit size).

8 Software

8.1 Drivers

Drivers currently are available for WIN2000 and WIN XP and for Linux. Both drivers have an application interface compatible to the drivers made for the SOHARD (http://www.sohard.de) Arcnet cards. So it´s easy to use PM20100 *or* COM2002x controllers by simply changing the driver.

8.2 Hints for programmers

The PM20100 is fairly easy to operate but especially the interrupt handling should be done with some care. Please observe the following hints to avoid spurios and unexpected data corruption and in the consequence an unnecessary loss of life time for the poor guy in charge to debug these kind of errors.

8.2.1 Interrupts

- Interrupts are critical while happening during a CMD transfer.
  Make sure that an interrupt can not interrupt a write PAR - write CMD sequence, if a CMD with a parameter write access inside the interrupthandler itself is being used. The parameter value after the interrupt may have been overwritten after leaving the interrupthandler !

- Make sure to disable the RX interrupt prior to writing data into a page *outside* the interrupt handler if page data is read out *inside* the interrupthandler. Mixed write and read accesses to/from the PAGE_DATA register may cause data corruption because the internal ram address counter is changed by both write *and* read accesses.

- Please keep in mind, that after an interrupt has been cleared, the next interrupt may follow almost immediately (1 microsecond and shorter) afterwards. This happens, when the PM20100 has detected an event which has been enabled to trigger an interrupt. So please make sure the interrupthandler can handle this situation properly.

8.2.2 Example

The following example shows typical sequences required for initializing the PM20100, to transmit a packet and to receive a packet.

8.2.2.1 Initialization

The Node will have the id decimal 99 and will operate with 10 MBps:

Command	Parameter	Description
CMD_SET_BITRATE	0x09	Sets the Bitrate to 10 Mbps
CMD_SET_SID	0x63	Sets the Node ID to decimal 99
CMD_EN_ARC	xx	The PM20100 joins the network

8.2.2.2 Transmit a packet

A packet with 3 Bytes (values are 1,2,4) shall be transmitted from page 1 to the node with the ID decimal 128:

Command	Parameter	Description
CMD_SET_PAGE	0x01	Select page 1
CMD_SET_DID	0x80	Sets the Destination ID to decimal 128
--	--	Write three bytes of data (values 1,2,4) to the DATA register.
CMD_SET_TX_SID	0x63	Sets the SID. Only required in Bridge Mode (i.e. Virtual nodes are enabled)
CMD_SET_PAC_LEN_L	0x03	The packet length will be 3.
CMD_SET_PAC_LEN_H	0x00	
CMD_SET_EXNAK	0x17	After 128 NAKs the packet transmission automatically will be aborted if the receiver has no buffer available.
CMD_EN_PAC_TX	0x01	Enables page 1 for transmission

That´s it.
Check the status of the packet with the CMD_GET_PAGE_STS (PAR =0x01) command to find out whether the transmission was successfully or not. Of course the interrupt functions may be used as well (not shown here).

8.2.2.3 Receive a packet

A packet shall be received and stored in page 2:

Command	Parameter	Description
CMD_EN_PAC_RX	0x02	Enables page 2 for receiving

Check the status of the packet with the CMD_GET_PAGE_STS (PAR =0x02) command to find out whether a packet was successfully received or not. Of course the interrupt functions may be used as well (not shown here).

To read the received data:

Command	Parameter	Description
CMD_SET_PAGE	0x02	Prepare for reading the received data from page 2

If the status register indicates a received packet, you can start reading the data from the DATA register. The first byte is the Status byte, the second one the lowbyte of length, the third one is the highbyte of length, the fourth indicates either the page qualifier or the node id the packet is transmitted to (depends on the options enabled).
The following bytes represent the payload data. Read as much bytes as the length indicates.

9 Glossary

Abbreviation	Description
SID	Source Identifier [1]
FID	Frame Identifier [1]. The type of packet transmitted on the network
DID	Destination Identifier[1] The identifier of the node the packet data is transferred to.
ACK	Acknowledge [1]
NAK	Negative Acknowledge [1]
FBE	Free Buffer Inquiry [1]
PLL	Phase Locked Loop
CRC	Cyclic Redundancy Check. Here: 16 Bit Checksum to ensure PAC data integrity[1]
SoC	System-On-Chip
FPGA	Field Programmable Gate Array
FIFO	First-in-first-out

10 Open issues

- None known

11 Features planned

- Testfunctions for supporting SW Tests
-

12 References

Reference	Document
[1]	ANSI/ATA 878.1 Local Area Network Standard for Arcnet
[2]	Datasheet COM20022, Standard Micro Systems (SMSC), http://www.smsc.com
[3]	Datasheet PM20100
[4]	Datasheet DS2431, Dallas Semiconductor/MAXIM
[5]	WISHBONE System-on-Chip (SoC) Interconnection Architecture for Portable IP Cores, Revision B.3, Released September 7, 2002 , www.opencores.org

13 Contact Address

SOHARD Embedded Systems GmbH
Wuerzburger Str. 197
D-90766 Fuerth
Germany

Phone +49 (0)911 97341 - 500
Fax +49 (0)911 97341 - 510

Email: info@sohard.de
Web: http://www.sohard.de