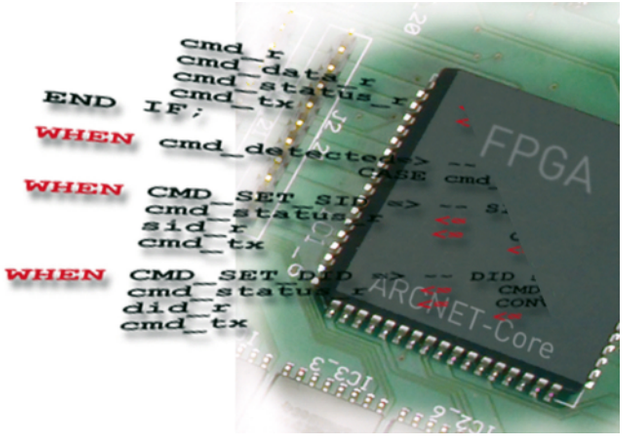
DATASHEET

SOHARD
EMBEDDED SYSTEMS

SH IP-CORE-ARCCTRL

ARCNET Network Controller as
IP Core for FPGA-based designs



Application & Functionality

The SH IP-CORE-ARCCTRL is an IP core that implements an ARCNET network controller for use in FPGAs (Field Programmable Gate Arrays). It is designed for and developed in VHDL. Portations exist for Altera and Xilinx FPGAs, it may easily be ported to FPGAs of other manufacturers.

The IP Core is completely compatible with the ARCNET standard.

Due to its flexible design is can be used for a wide field of applications:

- One-Chip PCI-Express ARCNET card
- Simple and cost-effective node for versatile digital I/O
- universal ARCNET-ARCNET or ARCNET-Ethernet bridge with virtual node-mapping
- Highspeed point-to-point connections
- Embedded networking
- System-On-Chip solutions

We use SH IP-CORE-ARCCTRL in our own products.

Key features

Compatible to ANSI/ATA 878.1 (Local Area Network Standard for ARCNET)
Up to 16 transmit/receive pages
Bitrates 19 kbit/s up to 10 Mbit/s
Automatic packet transmission abort after EXCNAK
Duplicate node detection
Different host-interfaces: - Classic host-interface 8 bit - AXI BRAM Interface
Receive-All Mode
Bridge function
Network node list
Easiliy portable to any FPGA types, e.g. Altera's Cyclone series, Xilinx' Zync 7000 platform ...
Easy in-field updates and upgrades

Order information

For further information including licensing options please contact us anytime.

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