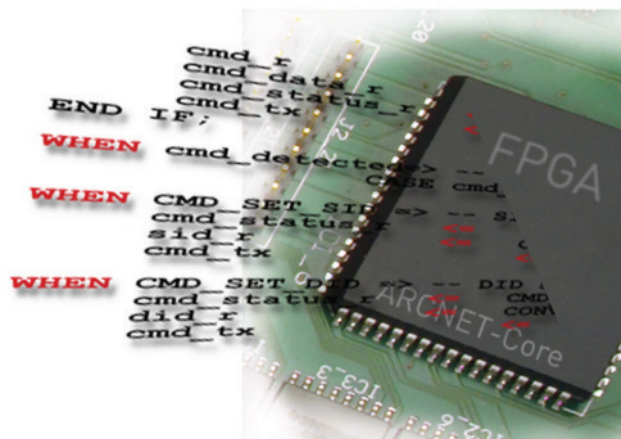


SH IP-CORE-ARCHUB

ARCNET hub IP core for FPGA based design



Scope of application

The maximum length of a network segment is limited by the transfer method used when implementing ARCNET networks. Amplifiers (hubs) can connect several segments in series to expand networks. However, bit jitter and the regeneration of signal levels and signal shapes are important in this case. Although common hubs regenerate signal levels they do not reduce but even increase bit jitter. In comparison to them the SH IP-CORE-ARCHUB regenerates signals and reduces bit jitter. With their very short transfer time of less than 3 bits, multiple SH IP-CORE-ARCHUB can be cascaded as long as the timeout conditions of connected ARCNET nodes are met.

Design & Functionality

The SH IP-CORE-ARCHUB is an ARCNET hub IP core that was designed for use in CPLDs and FPGAs. Due to use of VHDL, the design can be transferred easily to diverse CPLD and FPGA types from various manufactures such as Altera (MAX II, Cyclone and the Stratix series), and Xilinx (CoolRunner II, Spartan and Virtex series).

The IP core is completely compatible to ARCNET standards and can be used as replacement of SMSC Hub Controller TMC2005-xx. The SH IP-CORE-ARCHUB has already been used for long time in our market-proven product lines: SH ARC-Mx-HUB and SH ARC-HUB.

Diagnostic Features

The SH IP-CORE-ARCHUB can detect and report the multiple network events via LED's (see table "Diagnostic Features").

Key Features

- Fully compatible to ANSI/ATA 878.1 Local Area Network Standard for ARCNET
- Variable number of ports (3, 5, 8 and more)
- Automatic bit rate recognition and adaption
- Supported bit rates adjustable from 156.25 kbit/s up to 10 Mbit/s
- Two transmission modes: sine dipulse and backplane
- ARCNET signal regeneration
- Enhanced diagnostic features
- Design entirely written in VHDL
- May be easily adopted to other CPLD and FPGA types
- Easy in-field updates and upgrades

Diagnostic Features

Recon	Indicates the port receiving a RECON burst.
Alert burst error	Indicates ARCNET telegram headers deviating from the spec.
Lock	Indicates a correctly recognized data rate
HIT error	Indicates transceiver malfunction
Coax disable	Indicates disabled coaxial transmission provoked by inapt data rates to protect transceivers
TX-error	Indicates transmission errors due to unspecified data rates or non-comforming ARCNET nodes

Required Resources

The following table provides an overview of the resource usage on Altera Cyclone II (EP2C8) FPGA.

Resource	3 ports	5 ports	8 ports
Total logic elements	366 / 8,256 (4%)	393 / 8,256 (5%)	413 / 8,256 (5%)
Total combinational functions	365 / 8,256 (4%)	392 / 8,256 (5%)	412 / 8,256 (5%)
Dedicated logic registers	173 / 8,256 (2%)	180 / 8,256 (2%)	187 / 8,256 (2%)
Total registers	173	180	187
Total memory bits	8 / 165,888 (<1%)	8 / 165,888 (<1%)	8 / 165,888 (<1%)
Total pins	17 / 182 (9%)	27 / 182 (15%)	42 / 182 (23%)

The following table provides an overview of the resource usage on Xilinx Virtex4 (XC4VFX12) FPGA.

Resource	3 ports	5 ports	8 ports
Number of Slices	207 / 5472 (3%)	223 / 5472 (4%)	244 / 5472 (4%)
Number of Slice Flip Flops	175 / 10944 (1%)	182 / 10944 (1%)	192 / 10944 (1%)
Number of 4 input LUTs	388 / 10944 (3%)	415 / 10944 (3%)	453 / 10944 (4%)
Number of bonded IOBs	17 / 240 (7%)	27 / 240 (11%)	42 / 240 (17%)
Number of GCLKs	7 / 32 (21%)	9 / 32 (28%)	12 / 32 (37%)

Order Information

Please contact us for the order and further information about this product.