Manual

SOHARD
EMBEDDED SYSTEMS

SH IP-CORE-ARCCTRL

Enhanced ARCNET Controller for FPGA-based designs

Version 02.12.2

CONTENTS

1 Revision history

Version	*Change*
V. 02.12.2	- Various message descriptions updated
V. 02.12.1	- Revised Chapter 7 Implementation - Changed telephone number - Layout
V. 02.12	- Abort after EXNAKs fixed (3.1.1 Commands, IP-core V. 0.107) - Interrupt handling updated (9.1.1 Interrupts, IP-core V. 0.106) - Timeout values updated (9.1.2 Extended timeouts) - Prerequisite for feedback loop added (6.2 ARCNET Transceiver Interface) - Emulated nodes rephrased from virtual nodes (5 Bridge Mode)
V. 02.11	- Clarification on subcommands - Additional message descriptions - Formatting improved
V. 02.10	Clarification on messages
V. 02.09	- Revised descriptions of timeout commands - Added new chapter ‘Extended timeouts’
V. 02.08	- Changes in description of CMD_SET_PAGE - Changes in chapter 9.1.2.3 Receive a packet
V. 02.07	- Fixed misspelling - Better description of demo mode - Fixed description in AXI BRAM Interface (signal arcctrlif_data_out_o) - Better description of IRQ_STS registers. Added addition hint for programmers.
V. 02.06	- Excluded everything about 1-wire memory device support (obsolete license method) - Updated CMD Names and Command codes - Updated description of CMD register - Uniform number format of command codes and parameters - Correction of MSG_NAME register type - Various linguistic corrections
V. 02.05	Added Xilinx BRAM Interface
V. 02.04	Editorial update and Handling of Register MSG_NAME updated (V00.97 of IP-Core)
V. 02.03	Block diagram and pinning updated (V00.93 of IP-Core)
V. 02.02	License, Software and contact information updated
V. 02.01	- CMD_EN_TM and Recon Diagnostic Messages added (FPGA version >=V00.89) - Faster Access from Host controller (less wait states for signal wait_ext)
V. 02.00	CI update
V. 01.00	First officially released version

2 Overview

The SH IP-CORE-ARCCTRL is an ARCNET [1] controller designed for Field Programmable Gate Arrays (FPGAs). It is written in VHDL and was designed for Altera FPGAs (Stratix, Apex Cyclone and MAX10 families) and Xilinx FPGAs (Kintex 7, Spartan 3/3E, Virtex 2,4, Zynq). The design contains some Altera/Xilinx megafunctions like RAMs and FIFOs, which are clearly identified and have to be substituted when FPGAs of other vendors are used. Compared to classic „hardcoded“ ICs, the SH IP-CORE-ARCCTRL offers unlimited possibilities for the users to adapt the design to their needs.

3 Features

- Fully compatible to ANSI/ATA 878.1 Local Area Network Standard for ARCNET
- Up to 16 transmit/receive pages for long and short ARCNET packets
- Bit rates adjustable from 19 kbit/s up to 10 Mbit/s
- Automatic packet transmission abort after EXCNAK
- Token auto-repeat
- Improved network configuration
- Enhanced diagnostic functions
- Duplicate node detection
- Simple register-based interface
- Receive-All Mode (configurable)
- Bridge function with emulated nodes (configurable)
- Complete Network Node List (configurable)
- “Classic” bus interface
- Design entirely written in VHDL, except for RAM and FIFO functions only
- May be easily adapted to other FPGA types
- In-field updates and upgrades are simple
- Future-proof
- Free license for SH IP-CORE-ARCCTRL in Demo Mode (fix node-id)

3.1 Applications

Due to its high flexibility the design may be used for or adapted to a wide field of applications:

- One-Chip PCI ARCNET card (a free PCI Core is available from www.opencores.org)
- Simple and cost-effective node for versatile digital I/O
- Universal ARCNET- ARCNET or ARCNET-Ethernet bridge with emulated node-mapping
- High speed point-to-point connections
- Embedded networking
- System-On-Chip solutions

4 Host interface

The host interface is the interface to an external or internal microcontroller. It is very similar to an ISA-bus-like interface with read, write, chip select control signals, an 8-bit data bus and a 4-bit address bus.

4.1 Registers

Only a few registers are required to control the SH IP-CORE-ARCCTRL.

Name of Register	Address (hex)	Read/Write	Description
PAR	0	R/W	Parameter field for CMD. Must be set prior to executing a CMD which requires a parameter. Additionally, this register contains the return value of any CMD_GET_xx command. Note: 1) A write access to this register is ignored if the previous command has not been completed. 2) Writing to this register disables the interrupt temporarily. The interrupt is enabled again, when the CMD register is written to.
CMD	1	R/W	Writing to this register triggers the IP-CORE-ARCCTRL to execute the written command (see table of the commands). After-wards this register contains the status of the command execution: value 0xFF - command is still being processed other value - command execution is completed. The value equals to the code of the executed command. Note: 1) writing to the CMD register is ignored, if previous command has not been completed. 2) the execution status will be reported via message register.
PAGE_DATA	2	R/W	This register is used to read and write data from and to the selected data page (see command SET_PAGE). Any access to this register will automatically increment the address pointer (see registers ADDR_L and ADDR_H). The address of the data is set by the registers ADDR_L and ADDR_H.
reserved	3	-	reserved
ADDR_L	4	R/W	Lower byte of the address that points to the data on the selected page (see command SET_PAGE). The address pointer is incremented automatically with each write or read access to the PAGE_DATA register. The command SET_PAGE resets this value to 0x04.
ADDR_H	5	R/W	Upper byte of the address that points to the data on the selected page (see command SET_PAGE). The address pointer is incremented automatically with each write or read access to the PAGE_DATA register. The command SET_PAGE resets this value to 0x00.
IRQ_STS_PAC_ITPI	6	R	This register shows interrupts from data pages that are generated on completion of packet receipt and transmission. If enabled, each data transmission causes an interrupt. Bit 3..0

Name of Register	Address (hex)	Read/Write	Description
			contains the page index, Bit 7..4 the events. See Table IRQ_STS_PAC.
IRQ_STS_PAC_PS	7	R	This register contains the status of the transmission of the page that generated an interrupt (see IRQ_STS_PAC_ITPI)
IRQ_STS_SYS	8	R	Various events like Reconfigurations, etc. are recorded by this register. If enabled, each event causes an interrupt. See Table IRQ_STS_SYS.
MSG_PAR	9	R	Contains a parameter field for the MSG_NAME (see MSG_NAME)
MSG_NAME	A	R/W	The MSG_NAME register is supplied by an internal FIFO. The messages provide information on the internal status of the controller, network events and responses to CMDs (see 3.2). The message will be updated on write access. So the software needs to write any value to MSG_NAME in order to get the next message.
reserved	B..F		reserved

4.1.1 Commands

Receiving a command (and if necessary a parameter) the SH IP-CORE-ARCCTRL performs the required action like setting parameters, starting packet transmission, receptions and so on. If the command requires a parameter, this parameter must be written to the PAR register beforehand. Writing a command code to the CMD register, will cause the command to be executed.

Table: SH IP-CORE-ARCCTRL commands and parameters

CMD Name	Command code (hex)	Parameter (hex)	Description
CMD_SET_SID	01	01..FF	Sets the Node ID. Must be set prior to enabling the controller. Note: In Evaluation-mode the CMD_SET_SID command is ignored, and Node ID is hard-coded to 0x0A.
CMD_SET_EXNAK	07	00..1F	Bits 0..3 set the number of FBE-NAK sequences, after which the PAC_TX_EXNAK in the IRQ_STS_SYS register will be set (EXNAK = Excessive NAKs). Zero value for the bits 0..3 disables the transmission retries, for other values the number of retries will result in the power of 2 of the respective value (value 1 will result in 2 retries, 2 in 4 retries up to 15 resulting in 32768 retries). Bit 4 sets the EXNAK auto abort option: If enabled, an ongoing packet transmission will be aborted after EXNAK occurred and STS_PAC_ABORT will be issued in the STS_PAGE register. If disabled, the packet transmission will continue. Default after power-up or reset is 128 NAKs with auto-abort being disabled.
CMD_SET_BITRATE	08	00..09	Sets the ARNCET bit rate. 0 corresponds to 19 kBps, 1 to 38 kBps, 7 to 2.5 Mbps and so on up to 10 Mbps. Note: Setting the bit rate will automatically resets the ARCNET state machine, therefore it is recommended to set the bit rate directly after controller reset.
CMD_SET_DEBUG_LVL	0C	00..FF	Defines which kind of MSGs are stored in the MSG FIFO. Default value is 0x3F (all messages except for errors are disabled). Bit0=1: ignore ACK, NAK messages Bit1=1: ignore FBE messages Bit2=1: ignore messages of the type MSG_ITT Bit3=1: ignore messages of the type MSG_MY_ITT Bit4=1: ignore most messages except for any kind of error message Bit5=1: ignore all network messages like MSG_TOKENPASS_FAIL, MSG_NEXTID_FOUND etc.
CMD_GET_PARAM	29	[1]	This command allows to read the values of controller parameters (see Table “Subcommands”). The value may be read from the PAR register after the command was executed.
CMD_DIS_ARC	37	-	Disables the ARCNET transmitter of the controller. Parameters will not be changed. Packet transfers will be canceled. Some monitoring activity will still be active.
CMD_EN_ARC	38	-	Enables the ARCNET transmitter of the controller. The bit rate and the SID must have been set beforehand. The SH IP-CORE-ARCCTRL starts joining the network.
CMD_EN_BRDCST_RX	42	-	Enables the controller to receive Broadcast packets. Broadcasts are disabled by default.
CMD_DIS_BRDCST_RX	43	-	Disables the controller to receive Broadcast packets. Broadcasts are disabled by default.

[1]One of the subcommands described in the following section

CMD Name	Command code (hex)	Parameter (hex)	Description
CMD_RST_ARC	44	-	Resets the internal state machines. All network activity will be immediately stopped. All network-related parameters (except for the bit rate) need to be set again. A minimum waiting time of 20us is required, before the next read/write access.
CMD_RST_MSG_FIFO	45	-	The FIFO containing MSGs is being reset and all messages will be deleted.
CMD_EN_TM	46	-	Enables various features for testing an ARCNET network. Par=0x01: The next transmitted packets will contain an erroneous CRC Par=0x02: Tokens sent to this node will be ignored. This causes a reconfiguration sooner or later.
CMD_SET_ENHNCD_MODE	48	00..01	Bit 0: Enables/disables the Token Repeat function. If enabled, the token pass will repeated once, if the first try has failed. If disabled, the node will search for the next available node in the network as defined in [1] after one token pass has failed. Default is off. Bit 1..7 reserved for future expansions
CMD_REQ_NP_STS	4D	01..FE	Requests a status of the nodes that were detected by the controller in the range from the node ID defined by the parameter to 0xFF. After the request the SH IP-CORE-ARCCTRL will be incrementally processing its internal node list and reporting for detected nodes their node ID, status and node ID of the upper neighboring node. The request will be completed after 8 nodes were reported or the end of the list was reached. The command is only available, if the Bridge Mode option or the Network Node List option is enabled.
CMD_RX_ALL_EN	4E	-	Enables the Receive-All Mode. The command will be only available if the Receive-All option is enabled.
CMD_RX_ALL_DIS	4F	-	Disables the Receive-All Mode. The command will be only available if the Receive-All option is enabled.
Timeout Commands			
The timeout commands are only needed for extended timeout operation [1]. For timeout level-0, it's not necessary to change the counter values. The optimum counter values depend on the number of nodes in the network, the bit-rate and the run-time of the signal on the network lines. All counter values represent multiples of a given bit length. Therefore the counter value is independent from the data-rate. See also chapter 'Extended timeouts'. Please be careful to use the same timeout settings for all nodes in the network.			
CMD_SET_TMR_TLT_L	10	00..FF	Sets the lower byte of the counter for the Token Lost Timer. This counter value represents multiples of 2048 bit lengths. The register defaults to the standard timeout value (1025 = 840ms @2.5Mbps) [1].
CMD_SET_TMR_TLT_H	11	00..FF	Sets the upper byte of the Token Lost Timer.
CMD_SET_TMR_TIP_L	12	00..FF	Sets the lower byte of the counter for the **K-value** of the Identifier Precedence Timer. TIP=K*(255-ID)+3us. [1] The counter value represents multiples of 0.5 bit lengths. The register defaults to the standard timeout value (730 = 146 us @2.5Mbps) [1].
CMD_SET_TMR_TIP_H	13	00..FF	Sets the upper byte of the Identifier Precedence Timer.
CMD_SET_TMR_TAC_L	14	00..FF	Sets the lower byte of the Activity Timeout Timer. The counter value represents multiples of 0.5 bit lengths. The register defaults to the standard timeout value (425 = 85 us @2.5Mbps) [1].
CMD_SET_TMR_TAC_H	15	00..FF	Sets the upper byte of the Activity Timeout Timer.
CMD_SET_TMR_TRP_L	16	00..FF	Sets the lower byte of the counter for the Response Timer. This counter value represents multiples of 0.5 bit lengths. The register defaults to the standard timeout value (383 = 76.6 us @2.5Mbps) [1].
CMD_SET_TMR_TRP_H	17	00..FF	Sets the upper byte of the Response Timer

CMD Name	Command code (hex)	Parameter (hex)	Description
Interrupt Commands			
CMD_SET_IRQ_MASK_PAC	09	00..FF	Enables interrupt sources. See table for IRQ_MASK_PAC
CMD_SET_IRQ_MASK_SYS	0A	00..FF	Enables interrupt sources. See table for IRQ_MASK_SYS
CMD_CLEAR**_IRQ_SYS**	0B	00..FF	Resets the IRQ_STS_SYS bits if the corresponding bit in the parameter field is set. The interrupt output is set inactive, if all bits in the IRQ_STS_SYS and IRQ_STS_PAC are cleared.
CMD_CLEAR_IRQ_PGE	0D	00..FF	Resets the IRQ_STS_PAC bits if the corresponding bit in the parameter field is set. The interrupt output will be disabled, if all bits in the IRQ_STS_SYS and IRQ_STS_PAC are cleared.
PAGE Commands			
CMD_SET_PAGE	18	00..0F	Sets the current page. All subsequent CMDs regarding packet transfers refer to this page. Bits 0..3 of the parameter field indicate the page index. **Note:** Writing or reading to the page via the PAGE_DATA register *always starts* (after CMD_SET_PAGE) at an internal offset of 4 bytes referred to the beginning of the page. The first four bytes of the page are reserved for internal purposes for transmission. This must be taken in account, if a RAM test shall be performed Preparing a packet for transmission: First select the page (CMD_SET_PAGE). Then simply write the data to the PAGE_DATA register. DID, packet length and SID (in Bridge Mode only) must have been set by the appropriate commands before starting the transmission with the EN_PAC_TX command. To make sure that a previous transmission from this page has been completed, the status of the page should be checked beforehand. Reading a received packet: If the information about the length, SID or DID of the received packet is necessary, the page address should be set to 0 (ADDR_L=0) after CMD_SET_PAGE. The data structure is: Address 0: STS_PAGE Address 1: LSB of packet length Address 2: SID Address 3: DID Address 4: Start of payload To make sure the data is valid, the STS_PAGE register should be evaluated first. Please note, that the DID is not valid, if a broadcast packet has been received.
CMD_SET_DID	02	00..FF	Sets the Destination ID for a packet transmission to another node in the network. 0 means the packet will be transmitted as a broadcast packet. Refers to the page selected by the CMD_SET_PAGE command.
CMD_SET_TX_SID	19	01..FF	Sets SID for the data packet in selected data page (5).
CMD_SET_PAC_LEN_L	05	00..FD	Sets the lower byte of the length of a data packet to be sent. Refers to the page selected by the CMD_SET_PAGE command. **Note:** packet with lengths of 254 – 256 and > 508 are not allowed.
CMD_SET_PAC_LEN_H	06	00..01	Packet length is >= 257 byte (if set to 1), otherwise 1..253 according to the CMD_SET_PAC_LEN_H command Refers to the page selected by the CMD_SET_PAGE command.
CMD_EN_PAC_TX	35	00..0F	Enables a packet transmission and defines the selected page as a transmit page. All required parameters like DID, LEN and packet

CMD Name	Command code (hex)	Parameter (hex)	Description
			data must have been set before executing this command. The parameter field indicates the selected page. Be aware, that the transmission will only take place, if an ongoing transfer has been completed and no other pages had been enabled before. The packets are transmitted in the same order, as they have been enabled.
CMD_EN_PAC_RX	40	00..0F	Enables a page for receiving and defines the selected page as a receive page. The parameter field indicates the selected page. Be aware, that the reception takes place only, when an ongoing running transfer has been completed and no other pages had been enabled before. The packets are stored on the selected page in the same order as they have been enabled.
CMD_DIS_PAC_RX	41	00..0F	Disables a page from receiving. The parameter field indicates the selected page. If the page was activated before for receiving, the STS_PAGE Register will show an STS_PAC_RX_ABORT condition. Otherwise this register will only be cleared.
CMD_GET_PAGE_LEN	25	00..FF	Gets the lower byte of the data length on the selected data page. The upper byte is encoded in the page status (see Table)
CMD_GET_PAGE_STS	27	00..0F	Gets the current status of a page. See table STS_PAGE. The parameter field indicates the selected page. The return value will be stored in the PAR Register
CMD_ABORT_TX_PAC	36	-	Aborts a packet transmission. This command is executed only if the current PAC is not being transmitted.
Bridge Commands (4)			
CMD_VN_EN_NODE	49	01..FF	Enables an emulated node. After this command the SH IP-CORE-ARCCTRL acts like an ARCNET node with the node ID given in the parameter field.
CMD_VN_DIS_NODE	4A	01..FF	Disables an emulated node.
CMD_VN_EN_RX	4B	01..FF	Enables an emulated node for receiving packets. Note: To receive packets, the standard procedure for receiving packets (CMD_EN_PAC_RX etc.) has to be additionally performed.
CMD_VN_DIS_RX	4C	01..FF	Prevents an emulated node from receiving packets. The emulated node will answer FBE queries by NAK.

(1) depends on the FPGA used and the applied clock frequency.
(2) '-' means “Don´t Care”.
(3) All timing values and bit rates refer to an external clock of 40 MHz.
(4) The command is only available, if the Bridge Mode option is enabled.

4.1.1.1 Subcommands

Subcommands are used for the CMD_GET_PARAM commands.

Table: Subcommands for the CMD_GET_PARAM command

Subcommand Names	Subcommand (hex)	Description
PAR_NID	01	The node ID of this node.
PAR_EXNAK	07	For the description see CMD_SET_EXNAK command
PAR_BITRATE	08	The adjusted bit rate.
PAR_IRQ_MASK_PAC	09	See CMD_SET_IRQ_MASK_PAC command
PAR_IRQ_MASK_SYS	0A	See CMD_SET_IRQ_MASK_SYS command
PAR_NEXTID	39	The node ID of the upper neighboring node (next node ID). Will be 0, if there is no neighboring node or if the network is currently reconfiguring.

Subcommand Names	Subcommand (hex)	Description
PAR_NWRK_STS	3A	Bit 0 = 1 indicates a node in the network with the same node ID as this present node. In this case the command CMD_EN_ARC should never be executed, as duplicate node IDs will cause malfunctions in a network. Bit 1= 1 means no activity on the network, i. e. no other node is active. Bit 2 = 1 means a network with only one node has been detected. Bit 3 = 1 means some tokens have been detected. All bits will be reset by a CMD_DIS_ARC, CMD_SET_SID or CMD_RST_ARC command. Bit 4 = 1 means the network is stable (Reconfiguration finished, regular token-passing and data traffic). The bit is valid only, if the Bridge Mode option or the Network Node List option is enabled. Bit 5 = 1 means the netmap is ready
PAR_FPGA_VENDOR_ID	40	Vendor of the FPGA: 0 = Altera, 1= Xilinx, 2= Actel, others for future use
PAR_FPGA_FAMILY_ID	41	FPGA family: Altera: 0 = Cyclone, 1= Stratix, 2 = Apex, 3 = Cyclone II, 4 = Cyclone IV Xilinx: 0 = Spartan, 1 = Virtex
PAR_PM_ID_L	42	The individual product ID (lower byte) for the customer whom the IP-Core was compiled for. 00 = unknown
PAR_PM_ID_H	43	The individual ID (upper byte) for the customer whom the IP-Core was compiled for. 00 = prototypes, 01 = SOHARD Embedded Systems GmbH, 02 .. 04 = reserved, others are available on request.
PAR_VER_MAJOR	44	Version, upper byte
PAR_VER_MINOR	45	Version, lower byte
PAR_NR_OF_PAGES	46	Indicates the number of TX/RX pages available. The maximum value is 16 and depends on the type of FPGA the design was compiled for.
PAR_SYS_RSRC	47	Bit 0: Message FIFO is enabled/disabled Bit 1: CMD_SET_TMR_xx commands enabled (if disabled the built-in default values will be used) Bit 2: Network Status detection is enabled/disabled Bit 3: Enhanced Mode functions enabled. See CMD_SET_ENHNCD_MODE command. Bit 4: Fast Host interface. If 1, the interface will be clocked with the external clock, otherwise with half of the external clock. Bit 5: Bridge Mode. If 1, the Bridge Mode is enabled, and emulated nodes are available. Bit 6: Network Node List. The complete Network Node List is available using CMD_REQ_NP_STS commands. Bit 7: If 1, Demo Mode is enabled. In Demo mode the CMD_SET_SID command is not being executed. This means the node ID of the SH IP-CORE-ARCCTRL is fixed to the default value 0x0A . 1 means enabled, 0 disabled.
PAR_ENHNCD_MODE	48	Bit 0 = 1: the Token Repeat function is enabled. See CMD_SET_ENHCD_FCKTS. Bits 1..7 = 0 (reserved)
PAR_SYS_RSRC1	49	Bit 0: Receive-All Mode is enabled/disabled Bits 1..7: reserved 1 means enabled, 0 disabled.

4.1.2 Status registers

The status registers show events that recently occurred. If enabled by the SET_IRQ_MASK_PAC or SET_IRQ_MASK_SYS command an event triggers an interrupt. Please note that you may not immediately see all occurred events at once and have to clear older events first, before seeing other events (see also chapter ‘Hints for programmers’).

4.1.2.1 IRQ_STS_PAC_ITPI Register

Name	Bit	Description
Page index	3..0	The page number to which the event refers.
PAC_TX_END	4	The transmission of a packet has been completed. Whether the transmission was successful or not may be retrieved via the CMD_GET_PAGE_STS command.
PAC_RX_END	5	A data packet has been received. Whether the reception was successful or not may be retrieved via the CMD_GET_PAGE_STS command.
reserved	6..7	reserved

Each bit may be reset individually by a CMD_CLEAR_IRQ_PGE command, if the corresponding bit in the parameter field is set.

4.1.2.2 IRQ_STS_PAC_PS Register

This register contains the status of the page that is referenced in the IRQ_STS_PAC_ITPI register (for details see Table STS_PAGE Register).

4.1.2.3 IRQ_STS_SYS Register

Event	Bit	Description
RECON	0	A reconfiguration burst has been triggered by this present node.
NEW_NEXT_ID	1	A new upper neighboring node (next node ID) has been detected.
PAC_TX_EXNAK	2	All FBEs for the packet transmission of a page have been declined by NAKs for the number of times set by CMD_SET_EXNAK.
MSG_BUF_HALF	3	The message buffer is half full.
MSG_ERROR	4	An error or warning has been stored in the Message FIFO.
NO_ACTIVITY	5	A “No Activity” condition has been detected. This usually occurs after a reconfiguration burst.
NW_CHANGE	6	The Network Node List has changed. The function is available only, if the Bridge Mode option or the Network Node List option is enabled.
reserved	7	reserved

Each bit may be reset individually by a CMD_CLEAR_IRQ_SYS command, if the corresponding bit in the parameter field is set.

4.1.3 IRQ MASK Registers

The interrupt mask registers enable or disable the various interrupt sources. They are controlled by the CMD_SET_IRQ_MASK_PAC / CMD_SET_IRQ_MASK_SYS commands.

4.1.3.1 IRQ_MASK_PAC Register

Name	Bit	Description
reserved	0..3	
PAC_TX_END	4	Enables interrupts for the following event: the transmission of a packet has been completed.
PAC_RX_END	5	Enables interrupts for the following event: A packet has been received.
reserved	6..7	

4.1.3.2 IRQ_MASK_SYS Register

Event	Bit	Description
RECON	0	Enables interrupts for the following event: A reconfiguration burst has been sent by this controller.
NEW_NEXT_ID	1	Enables interrupts for the following event: A new upper neighboring node has been detected
PAC_TX_EXNAK	2	Enables interrupts for the following event: All FBEs for the packet transmission of a page have been declined by NAKs for the number of times set by CMD_SET_EXNAK.
MSG_BUF_HALF	3	Enables interrupts for the following event: The message buffer is half-full.
MSG_ERROR	4	Enables interrupts for the following event: Message indicating the storage of an error or warning in the Message FIFO
NO_ACTIVITY	5	Enables interrupts for the following event: A “No Activity” condition has been detected. Usually occurring after a reconfiguration burst.
NW_CHANGE	6	Enables interrupts for the following event: The network has become stable or has become unstable (i. e. reconfigurations occur). This function is available only, if the Bridge Mode option or the Network Node List option is enabled. It may be used to trigger a read-out of the Network Node List via the CMD_REQ_NP_STS command.
reserved	7	

4.1.4 STS_PAGE Register

After a CMD_GET_PAGE_STS command the status of a page may be read from the PAR register. The table shows the possible status values. The status bits have different meanings if used as either a TX page or an RX page.

Table: STS_PAGE Register, when configured as a **transmit** page (PAGE_MODE Bit is set)

Name	Bit	Value (hex)	Description
PAC_LEN	0	0,1	0 means the packet contains up to 253 data bytes, 1 means it contains 257 data bytes or more.
PAGE_MODE	1	1	The page is configured as a TX page.
EN_PAGE	2	0,1	If 1, the page is enabled for transmission.
STS_IDLE	5..3	0	Reset value. If set, the page is waiting for being activated.
STS_PAC_PENDING	5..3	1	The page has been activated and will be transmitted as soon the receiving node is ready for reception.
STS_PAC_TX_OK	5..3	2	A packet has been successfully transmitted.
STS_FBE_TIMEOUT	5..3	3	A timeout after an FBE has occurred.
STS_PAC_TIMEOUT	5..3	4	A timeout after a PAC has occurred.
STS_PAC_ABORT	5..3	5	The packet transmission has been aborted by a command or by reaching the number of predefined NAKs, if the EXNAK auto abort option is enabled.
STS_PAC_ERROR	5..3	6	During the transmission of a packet an error has been detected and therefore the transmission has been aborted
STS_PAC_EXNAK	5..3	7	The number of NAKs set by the CMD_SET_EXNAK command has been reached. This value will only be issued for few clock cycles. If the auto abort option is enabled STS_PAC_ABORT will be issued instead.
reserved	6..7	-	For internal use

Table: STS_PAGE Register, when configured as a **receive** page (PAGE_MODE Bit is cleared)

Name	Bit	Value (hex)	Description
PAC_LEN	0	0,1	0 means the packet contains up to 253 data bytes, 1 means it contains 257 data bytes or more.
PAGE_MODE	1	0	Page is configured as an RX page.
EN_PAGE	2	0,1	Page is enabled for reception when set to 1.
STS_PAC_RX_IDLE	5..3	0	Reset value. If set, the page is waiting for being activated.
STS_PAC_RX_PENDING	5..3	1	The page has been activated to receive the next incoming data.
STS_PAC_RX_BUSY	5..3	2	The page is currently being filled with received data.
STS_PAC_RX_ERROR	5..3	3	An error occurred during receiving.
STS_PAC_RX_OK	5..3	4	A packet has been received successfully.
STS_PAC_RX_ABORT	5..3	5	A packet reception has been aborted by a CMD_DIS_PAC_RX command.
STS_PAC_RX_BRDCST	6	0,1	If set, a Broadcast packet was received.
reserved	7	-	For internal use.

All status values are automatically reset by a CMD_EN_PAC_TX or CMD_EN_PAC_RX command.

4.1.5 Page Queuing

If several pages for transmit or receive are in operation (are enabled) at the same time, it is important to know the sequence of enabling. Otherwise the packet sequence may be mixed up. The SH IP-CORE-ARCCTRL fully takes care of this task.
The pages are always filled with received data in the exact same order as the pages have been enabled. In the same way packets are transmitted in the same order as they have been enabled. Interrupts indicating the completion of a PAC receive or transmission are generated in exactly the same sequence.

For example: Page 4, 2 and 7 are enabled one after the other by the CMD_EN_PAC_RX command. The first received packet is then stored in page 4, the second in page 2 and the third one in page 7.

4.2 Messages

To ease debugging a message buffer is provided. Originally the message buffer was intended for the sole purpose of enhancing debugging. Over time other messages, e.g. for net map functionality, were added.
The message buffer is a FIFO (default size: 2048 messages), which contains all messages generated by internal functions. Reading the MSG register will cause to consume the top message (and make the next stored message to appear there). If the MSG register contains zero value, the FIFO is empty (see also 3.1 Registers).
Note: When the FIFO is full, new messages will be discarded. The type of messages stored in the FIFO may be controlled by the debug level. Please keep in mind that the response to a command may be delayed, because the command has to be processed at first which takes several cycles.
The parameter field contains further information. The codes used for the messages (MSG) are the same as the codes for the commands (CMD).

MSG Name	Value (hex)	Parameter (hex)	Type/ DBG_LVL	Description
CMD_xx	-	Command-status	info	Most commands listed in the command table return a status value, which indicates the status after execution. 0x02 (CMD_STS_OK) - The command was executed successfully. 0x04 (CMD_STS_REJECTED) - The command is valid, but could not be executed due to the internal state. For example: The CMD_EN_ARC command is discarded, if the SID has not yet been set. 0x09 (CMD_STS_UNKNOWN) - An invalid command has been detected and is being ignored.
MSG_RECON_TRANSMITTED	50	--	Bit 5	The controller has sent a reconfiguration burst.
MSG_NEXTID_FOUND	51	NID	Bit 5	The controller has found a new upper neighboring node in the network with the ID NID.
MSG_DID_ERROR	52	--	error	An ITT send to this controller has a wrong DID.
MSG_HEADER_LEN_ERROR	53	--	error	The header of a received ARCNET frame has the wrong length.
MSG_MY_FBE_RECEIVED	54	DID	info	An FBE to this present node has been received.
MSG_ACK_SENT	55	--	Bit 0	An ACK has been sent by this present node.
MSG_MY_ACK_RECEIVED	56	--	info	An ACK has been received and directed to this present node.

MSG Name	Value (hex)	Parameter (hex)	Type/ DBG_LVL	Description
MSG_NAK_SENT	57	--	Bit 0	A NAK has been sent by this present node.
MSG_MY_NAK_RECEIVED	58	--	info	A NAK has been received and directed to this present node.
MSG_TOKENPASS_FAIL	59	--	Bit 5	The token could not be passed to another node.
MSG_TIMEOUT	5A	--	info	A timeout occurred after the transmission of an ARCNET frame.
MSG_PAC_RX_SID	5B	SID	Bit 4	The SID of a received packet.
MSG_PAC_RX_DID	5C	DID	Bit 4	The DID of a received packet.
MSG_PAC_RX_LEN_L	5D	Length, low byte	Bit 4	The lower byte of the length of a received packet.
MSG_PAC_RX_LEN_H	5E	Length, high byte	Bit 4	The upper byte of the length of a received packet.
MSG_PAC_RX_CRC_OK	5F	--	Bit 4	The CRC of a received packet is o. k.
MSG_PAC_RX_CRC_ERROR	60	--	error	The CRC of a received packet is corrupt.
MSG_PAC_NO_CRC	61	--	error	The received packet did not contain a CRC.
MSG_PAC_RX_LEN_ERROR	62	--	error	The received packet did not contain as much data as indicated.
MSG_PAC_TX_LEN_ERROR	63	--	error	The transmitted packet did not contain as much data as indicated
MSG_PAC_TX_OK	65	--	Bit 4	The transmitted packet has successfully been transmitted.
MSG_PAC_TX_TMT	66	00	error	A timeout occurred after the transmission of a packet.
MSG_FBE_TX_TMT	67	00	error	A timeout occurred after an FBE has been sent.
MSG_PAC_TX_STARTED	68	--	Bit 4	The transmission of a packet has been started.
MSG_RX_UNKNOWN_ELEMENT	69	Frame ID	Bit 5	A received ARCNET frame could not be identified as a valid ARCNET frame.
MSG_FIFO_2ARC_FULL	6A		error	The internal FIFO of the state machine is full. Commands had to be discarded.
MSG_NO_ACTIVITY	6B		Bit 5	A timeout of the TAC Timer has occurred, which means a reconfiguration burst has been sent by a node in the network.
MSG_ITT	6F	DID	Bit 2	An ITT directed to another node has been detected.
MSG_MY_ITT	70	SID	Bit 3	An ITT directed to this present node has been detected. In Bridge Mode the SID is variable, otherwise fixed.
MSG_TMT_ITT	71	01..FF	error	After an ITT has been sent a Timeout was detected. The parameter is the node ID which caused the timeout.
MSG_FBE_SENT	72	00	Bit 1	An FBE has been transmitted.
MSG_PAC_TX_GEN_ERROR	73	00	error	An error after a PAC transmission has been detected.
MSG_PAC_RX_GEN_ERROR	74	00	error	An error during a PAC reception has been detected.
MSG_NP_STATUS	75	00..FF	netmap	The message is generated if a CMD_REQ_NP_STS has been executed. Non-present nodes are not shown. Bit 0: If set, the node is present in the network and is a “real” node. Bit 1: If set, the node is present and is an emulated node Bit 2: If set, the node is enabled for receiving. Bit 3,4: If > 0 the node is present and is a real node. If Bits 0 and 1 are cleared, the node is not adjacent to any of the SH IP-CORE-ARCCTRL's real or emulated nodes.

MSG Name	Value (hex)	Parameter (hex)	Type/ DBG_LVL	Description
				The command is available only, if the Bridge Mode option or the Network Node List option is enabled.
MSG_NP_NXTID	76	01..FF	netmap	Indicates the ID of the upper neighboring node (next node ID). This messages always follows an MSG_NP_STATUS message and is linked to it. A maximum of 8 messages are issued, if a CMD_REQ_NP_STS is executed. The net list is valid only if an MSG_NW_STABLE message has been detected before. To ensure the validity of the Network Node List, perform a check if all MSG_NP_NXTID values together reveal an unbroken chain of Next IDs.
MSG_NW_NOT_STABLE	77	-	Bit 5 netmap	The network configuration is changing. For example, if a node has left the network or a reconfiguration burst has been sent. The command is available only, if the Bridge Mode option or the Network Node List option is enabled.
MSG_NW_STABLE	78	-	Bit 5 netmap	The network configuration is stable after reconfiguration. The command is available only, if the Bridge Mode option or the Network Node List option is enabled.
MSG_RECON_SID	79	00..FF	info	The value is the ID of the node sending the reconfiguration burst or zero if this node could not be identified.
MSG_RECON_RCVD	7A	-	info	A reconfiguration burst has been detected.
MSG_RECON_VERSION	7B	00..FF	info	A reconfiguration burst with diagnostic data attached to it by another SH IP-CORE-ARCCTRL has been detected. The value is the lower byte of its IP-Core version (PAR_VER_MINOR).
MSG_FIFO_ARC2HST_FULL	7C	-	error	Indicates that the internal FIFO of the controller was full and some messages were discarded. Depending on the discarded messages the controller may behave unpredictably. In this case please ensure that debug messages (see CMD_SET_DEBUG_LVL) are disabled.
MSG_FIFO_HST2EXT_FULL	7D	-	error	Indicates that the controller failed to write messages into the message FIFO. This happens when the controller (with specified filter settings) generates the messages faster than the host reads these messages
MSG_REQ_NP_STS_COMPLETE	7E	00..FF	netmap	Indicates if status request for the node list is completed, i. e. no further messages MSG_NP_NID, MSG_NP_NXTID and MSG_NP_STATUS will be generated: 00 – the status request was completed as the end of the node list was reached. Otherwise – the status request is completed after 8 status messages. The value is the node ID that should be used by the next CMD_REQ_NP_STS call.
MSG_NP_NID	7F	01..FF	netmap	This message is generated on status request using CMD_REQ_NP_STS. The value reports the node ID from the node list, that has the corresponding status (see MSG_NP_STATUS) and its upper neighboring node (see MSG_NP_NXTID).
MSG_PAC_TX_ABORTED	80			A pending transmission has been aborted
MSG_NETMAP_READY	81		netmap	Netmap has been completed
MSG_TX_ITT	82			Token has been passed
MSG_1ST_ITT_AFTER_RECON	83	01..FF		ID of the node that starts reconfiguration, with a single node network the ID of the one node.
NULL	00	-	-	The FIFO is empty, i. e. no messages are available.

5 Bridge Mode

The Bridge Mode is an advanced feature which allows the user to couple different ARCNET networks (e.g. networks with different bit rates, timing settings, numbers of nodes etc.) in a transparent way. This mode makes use of emulated nodes.

“Real” nodes in one network are represented by emulated nodes (implemented by the SH IP-CORE-ARCCTRL) in the other network. A link of any kind (Ethernet with TCP/IP protocol, modem lines, RS232, etc.) couples the bridges connected to the respective ARCNET networks. One Bridge (containing an SH IP-CORE-ARCCTRL, a processor and a Bridge software) in each ARCNET network controls the emulated nodes.

Example:

A node with ID=1 in network A “intends” to send a packet to the node with ID=2 in network B. The two bridges in the networks A and B then automatically set up an emulated node with ID=2 in network A and an emulated node with ID=1 in network B.

The node with ID=1 in network A then sends is packet to the emulated node with ID=2 in network A. The data is transferred from Bridge A to Bridge B. The emulated node with ID=1 in network B then sends the ARCNET data to the node with ID=2 in network B.

The Bridges must manage the enabling/disabling of the emulated nodes according to the status of the corresponding nodes in the other network, the communication between the bridges, the queuing of packets and so on.

6 Input / Output Pins

There are several groups of pins. They are divided into system pins (clock, reset, leds), pins for connection the ARCNET transceiver (rx, txenable etc.) and pins for connection to an external micro-controller.

6.1 System Interface

Table: Pins

Pin name	Direction	Description
clock_i	I	The master clock of 40MHz.
reset_i	I	Reset all internal logic
arcctrlif_int_o	O	High-active interrupt.
arcif_led_hst_no	O	Output for an LED. Every access (read or write) to the SH IP-CORE-ARCCTRL triggers the LED for about 3 ms.
arcif_led_act_no	O	Output for an LED. Reflects the signal activity on the “rxin” pin.

Note: O= Push-Pull Output, I = Input, IO = Input/Output

6.2 ARCNET Transceiver Interface

Table: Pins

Pin name	Direction	Description
rxin	I	The data received from the network (high-active).
npulse1	O	The /pulse1 output for ARCNET dipulse transceivers (low-active).
npulse2	O	The /pulse2 output for ARCNET dipulse transceivers (low-active).
ntxdata	O	The /txdata output to ARCNET transmitters using e.g. RS485 and fiber optics (low-active).
tx_en	O	Enables the ARCNET transmitter (low-active).

Note: O= Push-Pull Output, I = Input, IO = Input/Output

Please note: for the IP-Core to operate correctly it is essential that there is a feedback loop between the transmission path (npulse1 and npulse2 or ntxdata) and rxin.

Such a feedback loop is inherent to half-duplex ARCNET transmission techniques like sine-dipulse or RS485 which share one transmission line.

However, for optical transmission techniques which feature separated transmission lines for each direction, a feedback loop must be implemented between ntxdata and rxin by the hardware environment of the IP-Core.

6.3 Classic Interface

The following pins are provided as interface to a host (for example a micro-controller):

Table: Pins

Pin name	Direction	Description
arcctrlif_polarity_i	I	Defines the polarity of CS, RD and WR signals: 1 – Signals are high-active 0 – Signals are low active.
arcctrlif_cs_i	I	The chip select signal from the host. Enables write and read accesses.
arcctrlif_rd_i	I	The read signal from the host for read access. Timing requirements: - must be started 25 ns after address bus was set - minimal duration 50 ns - host must wait at least 350 ns before next IO access started, if the “wait_ext” is not being used
arcctrlif_wr_i	I	The write signal from the host for write access. Timing requirements: - must be started 25 ns after address bus was set - minimal duration 50 ns - host must wait at least 350 ns before next IO access started, if the “wait_ext” is not being used
wait_ext	O	If high, the SH IP-CORE-ARCCTRL is busy and cannot react to further read and write signals. The signal will be go low as soon as “rw_end” is active and the read/write signal is disabled.
rw_end	O	If high, the current read or write process is complete and the corresponding read or write signal may be deactivated. The host should not start the next read/write cycle until “rw_end” is high.
arcctrlif_data_in_i[7..0]	I	Data bus from host to SH IP-CORE-ARCCTRL
arcctrlif_data_out_o[7..0]	O	Data bus from SH IP-CORE-ARCCTRL to host
arcctrlif_addr_i[3..0]	I	Address bus from host

Note: O= Push-Pull Output, I = Input, IO = Input/Output

6.4 AXI BRAM Interface

For simpler interconnection with a ZYNQ the AXI BRAM interface was added.

Table: Pins

Pin name	Direction	Description
arcctrlif_en_i	I	BRAM Port enable signal.
arcctrlif_wr_i	I	BRAM Port write enable signal. Any non-zero value triggers the writing of the lower 8 bits.
arcctrlif_addr_i	I	BRAM Port address bus. The lowest 2 bits are ignored. Therefore registers will be accessed as reg[0] under adddress 0x0, reg[1] under adddress 0x4 and etc.
arcctrlif_data_in_i	I	BRAM Port write data bus. Only the lower 8 bits are used.
arcctrlif_data_out_o	O	BRAM Port read data bus. Only the lower 8 bis are used.

Note: O= Push-Pull Output, I = Input, IO = Input/Output

7 Implementation

7.1 Intel (formerly: Altera) FPGAs

7.1.1 Development Tool

The current design was developed using the Intel Quartus Prime Lite 17.1.

7.1.2 Resources

The following table gives a rough overview about the resources the design requires. The values refer to the Intel MAX 10 Family. Various options are available to reduce the use of resources.

Table: Resource count

Configuration	Logic Elements	Registers	Memory Bits
Default Design	6000	2300	111000

7.2 Xilinx FPGAs

7.2.1 Development Tool

The current design was developed with the Xilinx Vivado 2017.4.

7.2.2 Resources

The following table gives a rough overview about the resources the design requires. The values refer to the Xilinx Kintex 7 Family. Various options are available to reduce the use of resources.

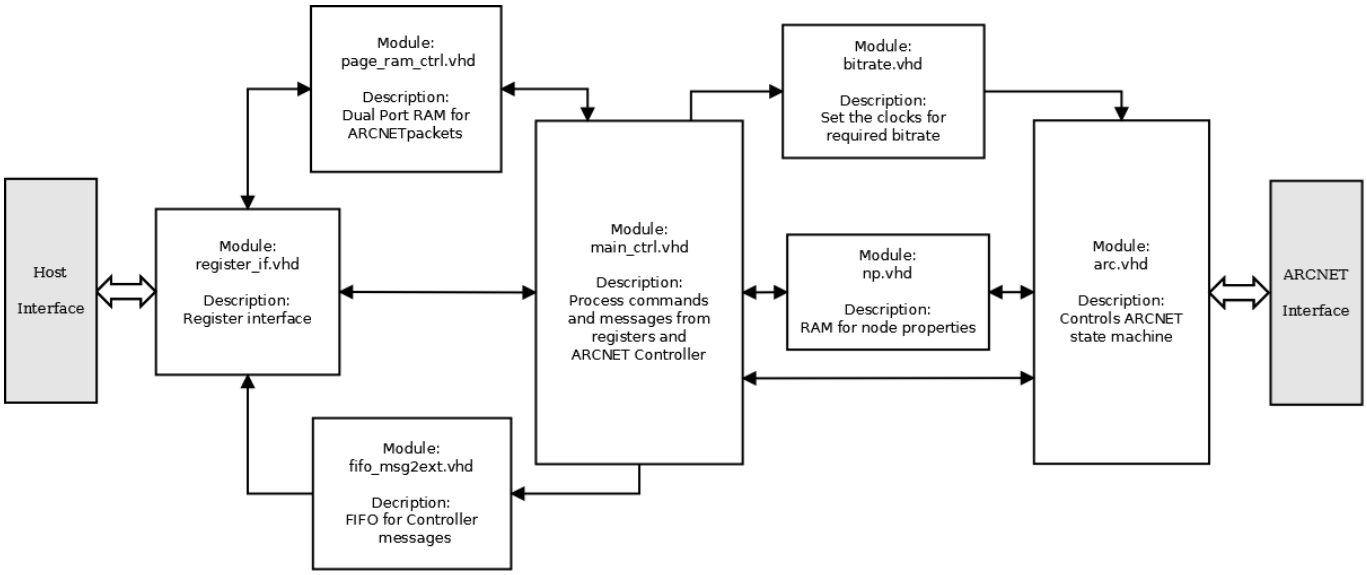
Table: Resource count

Configuration	LUT	FF	BRAMs
Default Design	3300	2200	6

8 Technical background information

The design has been completely written in VHDL for Altera FPGAs. However, it still relies on vendor-specific functions such as RAMs and RAM-based FIFOs. When the IP-Core is to be ported to FPGAs from vendors other than Altera, these components have to be replaced by equivalent functions.

The following sketch gives a general overview on the architecture of SH IP-CORE-ARCCTRL:



9 Software

The IP-Core described in this document is used in various SOHARD products. Thus SOHARD may provide support for the development of your system by advice as well as by providing a library with the SOHARD ARCNET RAW Interface.

9.1 Hints for programmers

9.1.1 Interrupts

The SH IP-CORE-ARCCTRL is easy to operate but especially the interrupt handling should be done with some care. Please observe the following hints to avoid unexpected behavior and data corruption:

- Interrupts are critical during a CMD transfer. For this reason, the host SW has to make sure that writing into PAR and CMD registers is not interrupted (and the PAR register potentially compromised before the command is executed). After a command has been written into CMD it will still require some time for execution. So you need to ensure that the previous command was completed before you start a new command. It is recommended that the host SW runs only one instance of the interrupt handler at a time.
- Please make sure that you do not use the SET_PAGE command inside the interrupt handler to prevent data corruption. For example, if you start to read data from page 0 and switch to page 1 in the interrupt handler, then you would continue to read from page 1 after completion of the interrupt.
- Please keep in mind, that after an interrupt has been cleared, the next interrupt may follow almost immediately (1 microsecond and shorter) after-wards. This happens, when the SH IP-CORE-ARCCTRL has detected an event which has been enabled to trigger an interrupt. So please make sure the interrupt handler can handle this situation properly.
- The Software always has to process all signaled interrupts in the interrupt status registers (IRQ_STS_PAC_ITPI and IRQ_STS_SYS) and finally clear them, to avoid missing an interrupt which has already been triggered but not yet signaled in the interrupt status registers. Sometimes interrupt events will only be signaled when older interrupts were cleared. Only if all bits in both interrupt status registers are ‘0’, the software has really processed all interrupt events. Use the interrupt status masks to disable interrupt events, which you do not want to process.

9.1.2 Extended timeouts

The SH IP-CORE-ARCCTRL offers the possibility to change some network timeout values. In most use cases the default values can be used. However, if the expansion of a network is very large and/or the data-rate is very slow, it could make sense to change the network timeout values. The optimum values depend on the number of nodes in the network, the bit rate and the run-time of the signal on the network lines. Common extended timeouts are defined and described in detail in the ARCNET specification [1]. The following table is showing the *recommended* counter values for the different timeout levels for the SH IP-CORE-ARCCTRL. Timeout level 0 is the standard/default level after reset. Changing the timeout values can be done using the timeout commands CMD_SET_TMR_… (see chapter 'Commands').

Name of Timer	Counter value for Timeout Level 0	Counter value for Timeout Level 1	Counter value for Timeout Level 2	Counter value for Timeout Level 3
TLT - Token Lost	1025	2050	2050	2050
TIP - Identifier Precedence	730	2872	5728	11560
TAC- Activity Timeout	427	1597	3157	6277
TRP – Response Timeout	381	1425	2817	5601

9.1.3 Examples

The following examples are typical sequences required for initializing the SH IP-CORE-ARCCTRL, to transmit a packet and to receive a packet.

9.1.3.1 Initialization

The node will have the ID 99 (0x63) and will operate at 10 Mbit/s:

Command	Parameter (hex)	Description
CMD_SET_BITRATE	09	Sets the bit rate to 10 Mbit/s
CMD_SET_SID	63	Sets the Node ID to 99
CMD_EN_ARC	-	The SH IP-CORE-ARCCTRL joins the network

9.1.3.2 Transmit a packet

A packet with 3 bytes (values are 1,2,4) shall be transmitted from page 1 to the node with the ID 128 (0x80):

Command	Parameter (hex)	Description
CMD_SET_PAGE	01	Select page 1
CMD_SET_DID	80	Sets the Destination ID to 128
--	--	Write three bytes of data (values 1,2,4) to the DATA register.
CMD_SET_TX_SID	63	Sets the SID. Only required in Bridge Mode (i.e. emulated nodes are enabled)
CMD_SET_PAC_LEN_L	03	The packet length will be 3.

Command	Parameter (hex)	Description
CMD_SET_PAC_LEN_H	00	Upper byte of the packet length is thus 0.
CMD_SET_EXNAK	17	After 128 NAKs the packet transmission will be aborted automatically if the receiver has no free buffer available.
CMD_EN_PAC_TX	01	Enables page 1 for transmission

That´s it.
Check the status of the packet with the CMD_GET_PAGE_STS (PAR =0x01) command to find out whether the transmission was successful or not. Of course the interrupt functions may be used as well (not shown here).

9.1.3.3 Receive a packet

A packet shall be received and stored in page 2:

Command	Parameter (hex)	Description
CMD_EN_PAC_RX	02	Enables page 2 for receiving

Check the status of the packet with the CMD_GET_PAGE_STS (PAR =0x02) command to find out whether the packet was successfully received or not. Of course the interrupt functions may be used as well (not shown here).

To read the received data:

Command	Parameter (hex)	Description
CMD_SET_PAGE	02	Prepare for reading the received data from page 2

If the status register indicates a received packet, you can start reading the payload from the DATA register. In most cases it’s also necessary to know the packet length, the SID or DID. This information is in the first four bytes of the page, which will be skipped by CMD_SET_PAGE!
To get this information, the page address has to be set back to 0 (set ADDR_L to 0 after CMD_SET_PAGE or set ADDR_L and ADDR_H to 0 and any time). See more details in the CMD_SET_PAGE description.

10 Glossary

Abbreviation	Description
SID	Source Identifier [1]
FID	Frame Identifier [1]. The type of packet transmitted on the network
DID	Destination Identifier[1]. The identifier of the node a token or payload data is sent to.
ACK	Acknowledge [1]
NAK	Negative Acknowledge [1]
FBE	Free Buffer Inquiry [1]
PLL	Phase Locked Loop
CRC	Cyclic Redundancy Check. Here: 16 Bit Checksum to ensure PAC data integrity[1]
SoC	System-on-Chip
FPGA	Field Programmable Gate Array
FIFO	First-in-first-out

11 Disclaimer

This manual and the interfaces, functions, operation codes and features it describes are subject to change.

12 References

Reference	Document
[1]	ANSI/ATA 878.1 Local Area Network Standard for ARCNET
[2]	***Datasheet COM20022, Microchip Technology, Inc. (former Standard Micro Systems SMSC), http://www.microchip.com***

13 Licensing

For questions on licensing options please contact info@sohard.de or any SOHARD sales representative.

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